LCD MODULE

SPECIFICATION

Model:	UE020HV-RB40-L018A
Version:	V1.0
Date:	2020.05.08

Customer Confirmation 客户确认

Approved by	Notes

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VIEWE Confirmation 优奕确认

Prepared by	Reviewed by	Approved by

REVISION HISTORY

Revision 版本号	Date 日期	Contents of Revision Change 修改内容	Remark 备注
V1.0	2020.05.08	Preliminary release	All

TABLE of CONTENTS

1. GENERAL INFORMATION

1.1 Features

1) Pixel Arrangement：RGB Vertical Stripe
2) Interface Mode：3 wire SPI + RGB 18Bits
3) Driver IC：ST7796HV
4) Operation Temperature：-20~70℃
5) Storage Temperature：-30~80℃
6) Backlight Type：White LED
7) Display mode： Normally White,
8) Pixel Density：212 PPI
9) LED life time：30,000 Hours

1.2 Mechanical Specification

Item 项目	Specification 规格	Unit 单位	Remark 备注
Pixel Driving element	IPS TFT	-	-
Screen Size	2.0	Inch	Diagonal
Resolution	320(W)*3(RGB)*280(H)	Dots	
Interface	3 wire SPI+RGB 666	-	18bit
Module Power Consumption	0.3	Watt	Typ.
Active Area	51.6(Φ)	mm	-
Pixel pitch (W*H)	0.16125(W)*0.16125(H)	mm	-
Module Size (W*H*D)	55.45(W)*59(H)*2.7(D)	mm	-
Luminance	300	cd/m^2	Typ.
Viewing Direction	ALL	O'clock	-
Display Color	262K	Colors	-

2. ABSOLUTE MAXIMUM RATINGS

Item 项目	Symbol 符号	Min. 最小值	Max. 最大值	Unit 单位	Remark 备注
Power supply1 voltage	VDD	-0.3	4.6	V	Note1
Power supply2 voltage	VDDI	-0.2	4.6	V	
LED forward current	I_F	-0.001	20	mA	For each led,Note1
LED Reverse Voltage	V_R	-	5	V	For each led,Note1
Operating temperature	T_{op}	-20	70	℃	(4Hours)Note1,2
Storage temperature	T_{st}	-30	80	℃	(4Hours)Note1,2
Humidity	H_{st}	10	90	%RH	Note1,3

(Ta=+25°C,GND=0V)

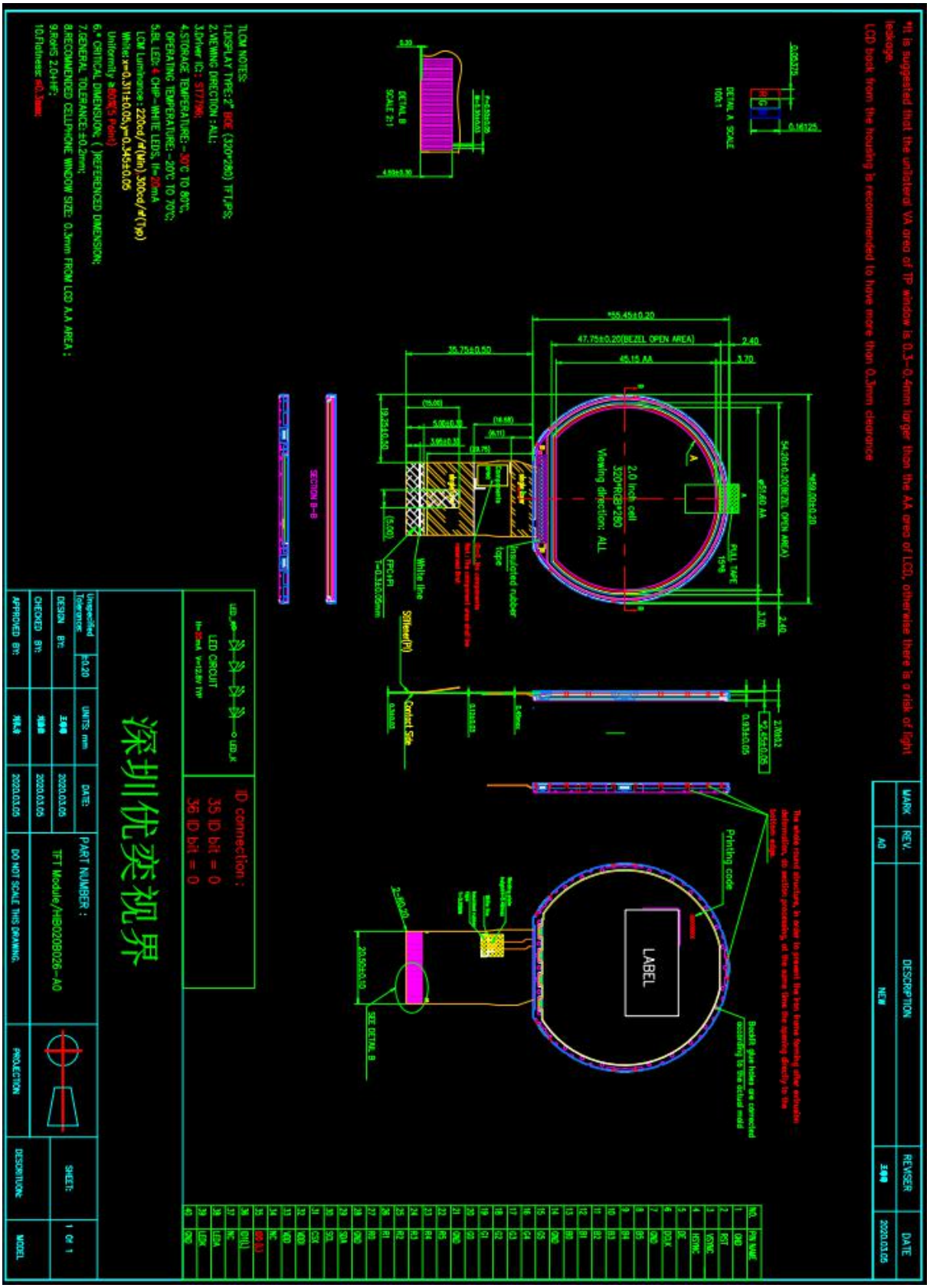
Note1:If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also if the module operates with the absolute maximum ratings for a long time, the reliability may drop.

Note2: In case of temperature below 0℃,the response time of liquid crystal (LC) becomes slower and the color of panel darker than normal one.

Note3: Temp. ≤ 60℃ , 90% RH MAX.

Temp. ＞60℃ , Absolute humidity shall be less than 90% RH at 60℃.

3. MECHANICAL DRAWING



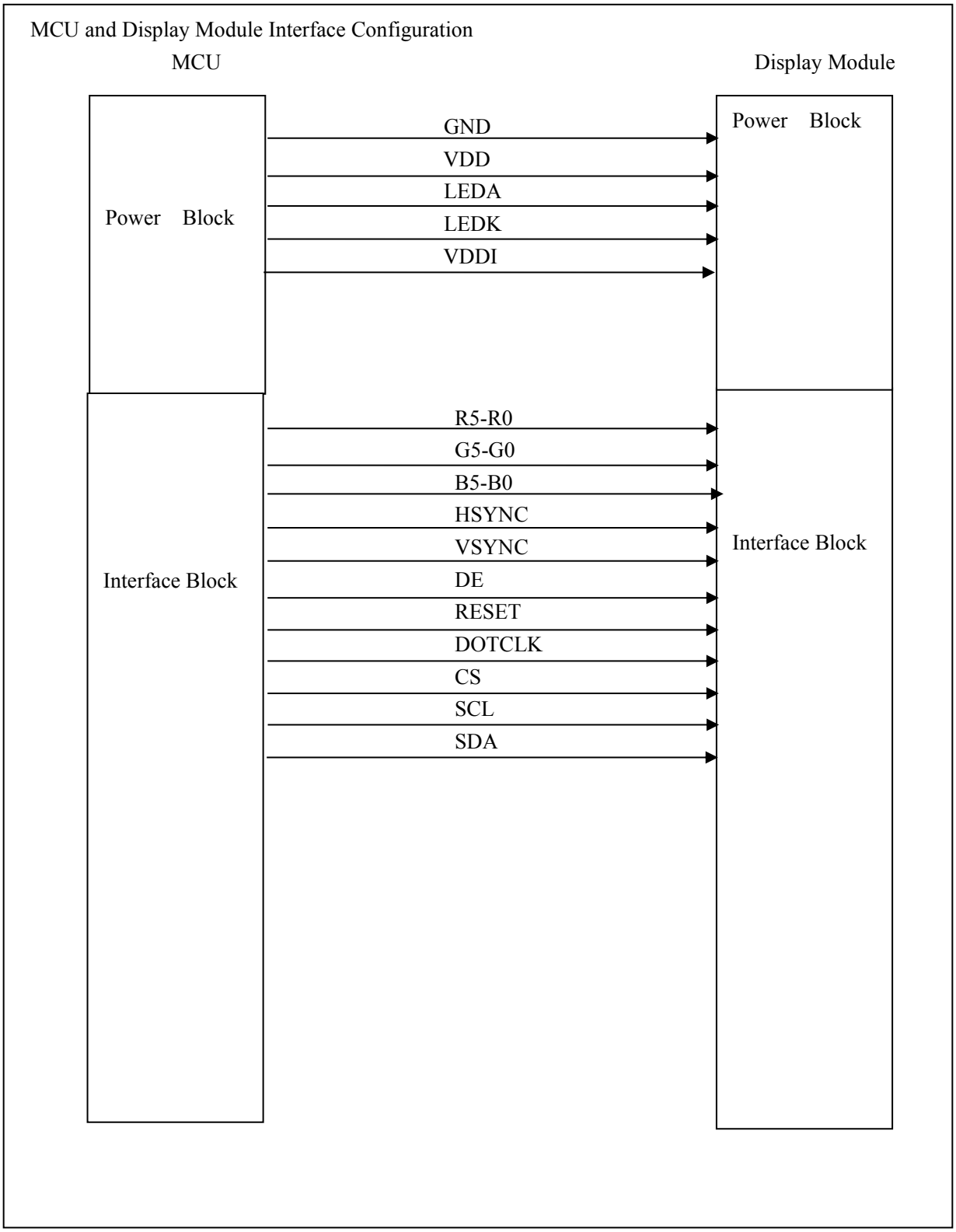
4. I/O CONNECTION & BLOCK DIAGRAM

4.1 I/O Connection

Pin No. 序号	Symbol 符号	I/O	Description 描述
1	GND	P	Power Ground
2	RST	I	The signal will reset the LCM, Signal is active low.
3	VSYNC	I	Vertical sync signal, Negative polarity
4	HSYNC	I	Horizontal sync signal, Negative polarity
5	DE	I	Data input enable. Display access is enabled when DE is “H”
6	DCLK	I	Dot clock signal for RGB interface operation
7	GND	P	Power Ground
8-13	B5-B0	I	Blue data input
14	GND	P	Power Ground
15-20	G5-G0	I	Green data input
21	GND	P	Power Ground
22-27	R5-R0	I	Red data input
28	GND	P	Power Ground
29	SDA	I/O	Data select pin for SPI interface
30	SCL	I	Clock select pin for SPI interface
31	CSX	I	Chip select pin for SPI interface
32	VDDI	P	Power supply to interface pins(1.8V)
33	VDD	P	Power supply for analog circuits
34	NC	-	No connected
35	ID0(L)	O	LCD ID0
36	ID1(L)	O	LCD ID1
37	NC	-	No connected
38	LEDA	P	Power supply for backlight anode
39	LEDK	P	Power supply for backlight cathode
40	GND	P	Power Ground

I：Input；O：Output；P：Power

4.2 Block Diagram



5. ELECTRICAL CHARACTERISTICS

5.1 TFT-LCD Panel Driving Section

Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Power Supply1 Voltage	VCC	2.6	2.8	3.3	V	-
Power Supply2 Voltage	IOVCC	1.65	1.8	2.8	V	
Normal mode	$I_{VDD+VDDI}$	-	12	16	mA	Note1
Sleep mode	$I_{VDD+VDDI}$		20	50	uA	
Logic Input High Voltage	V_{IH}	0.7VDDI	-	VDDI	V	-
Logic Input Low Voltage	V_{IL}	0	-	0.3VDDI	V	-
Panel Power Consumption	P_{VDD}	-	0.034	-	Watt	Note1
Module Power Consumption	P_{LCM}	-	0.3	-	Watt	Note1,2

(Ta=+25°C, DGND=AVSS=0V)

Note1:Measurement Conditions (Video Mode): Full Screen Red Pattern,VDD=3.3V,60Hz Refresh.

Note2: P_{LCM}= P_{VDD}+ P_{BL}， About P_{BL} information, inference to 5.2 Back Light Driving Section.

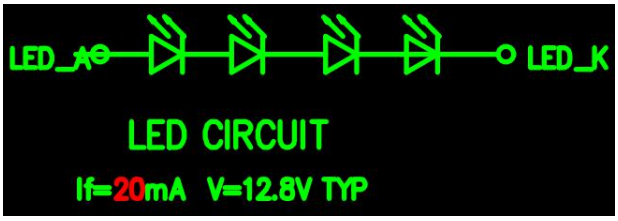
5.2 Back Light Driving Section

Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Forward Voltage	V_F	-	12.8	-	V	Note1
Forward Current	I_F	-	20	-	mA	Note1
Backlight Power consumption	P_{BL}	-	0.256	-	Watt	Note1
LED life time	-	30000	-	-	Hrs	Note2
LED Quantity			4		PCS	

(Ta=+25°C, DGND=AVSS=0V)

Note1: The LED driving condition is defined for each LED module (1LED Serial, 4 LED Parallel)。
For each LED ： IF=20mA,VF=3.2V(Typ.)/3.4V(Max.),Ta=25℃。

Note2:The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_{LED}=20mA(Per Led). The LED life time could be decreased if operating I_{LED} is larger than 20mA.



5.3 Power On/Off Sequence

VDDI and VDD can be applied in any order.

VDD and VDDI can be power down in any order.

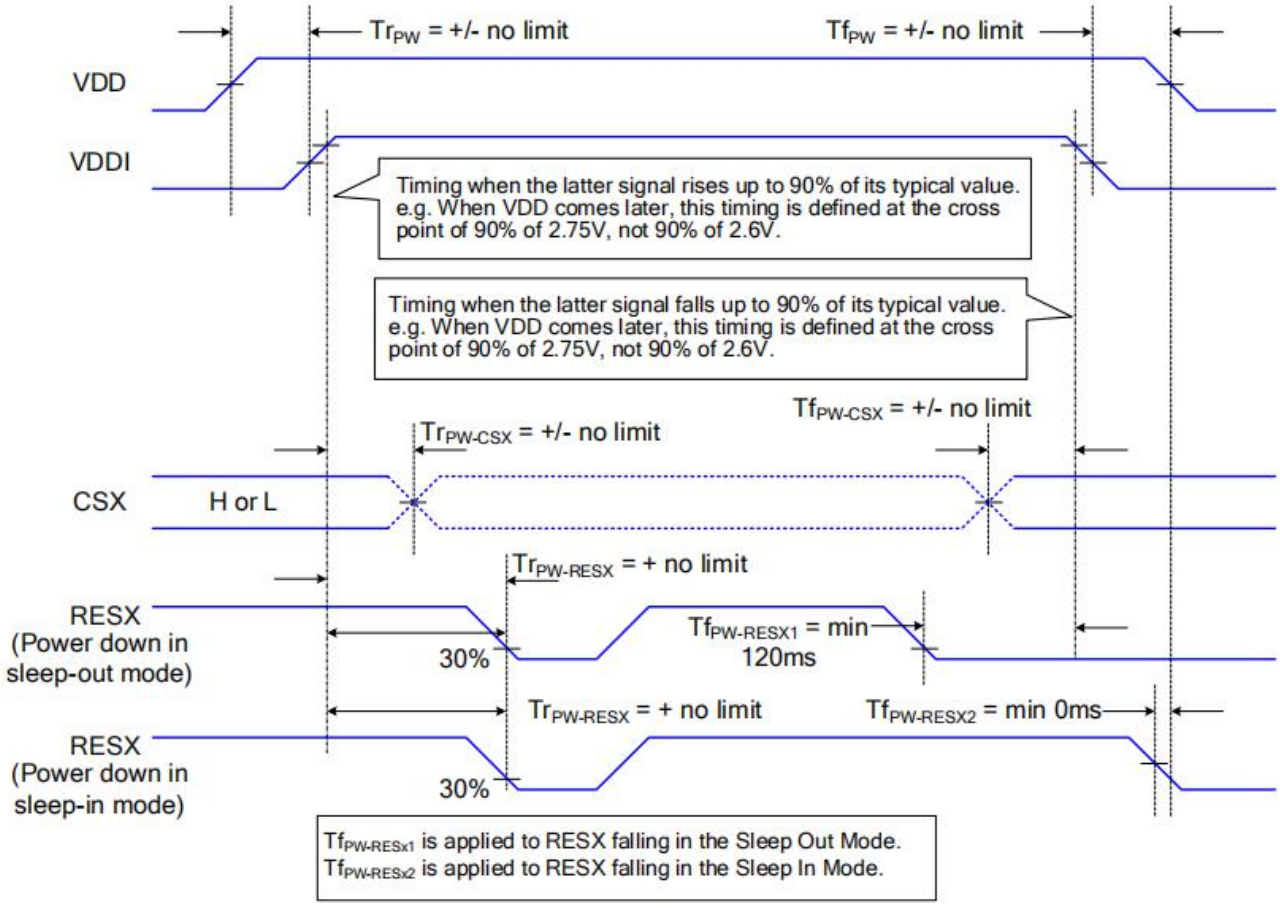
During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.
Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below

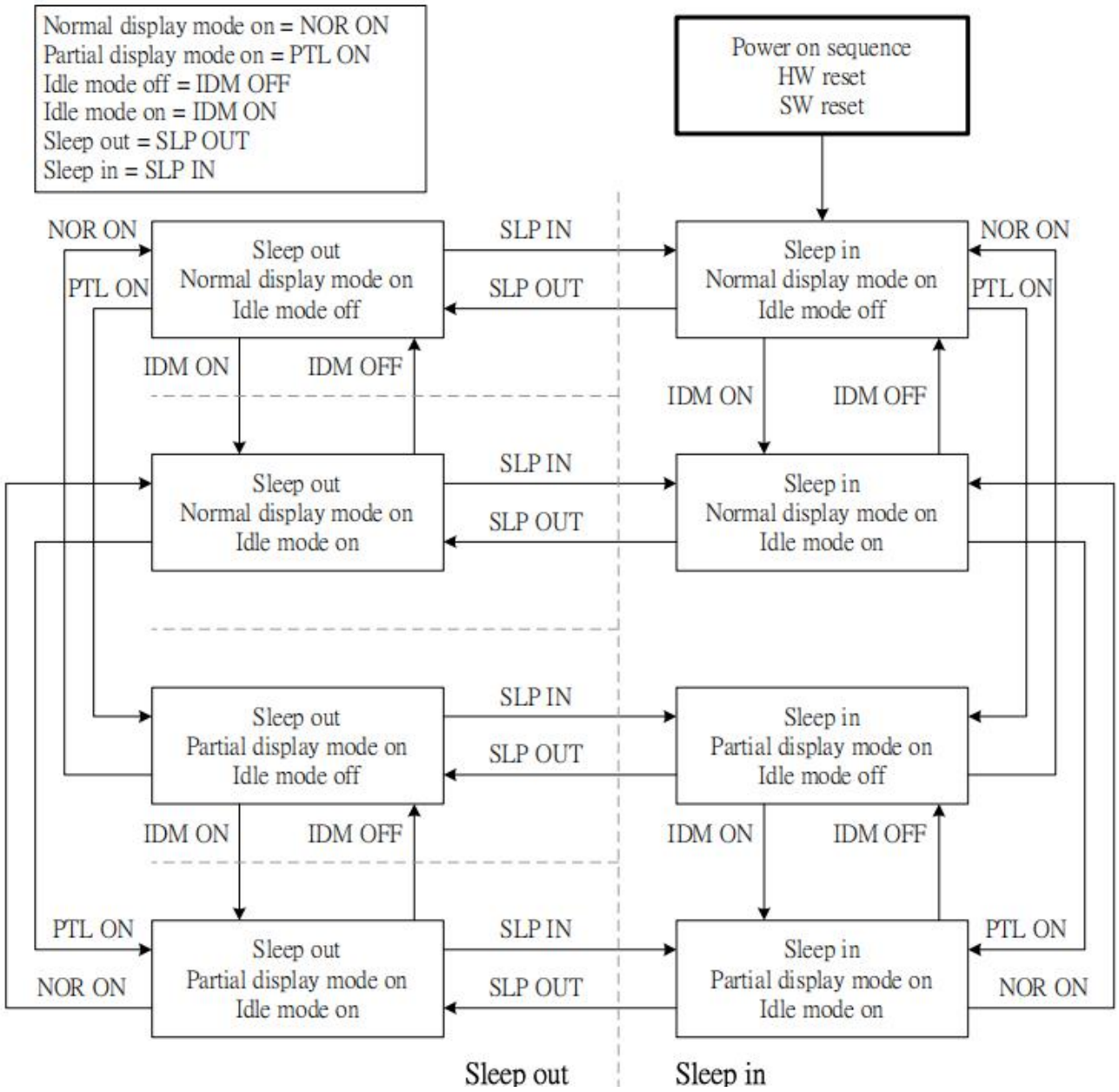


5.3.3 Uncontrolled Power Off

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

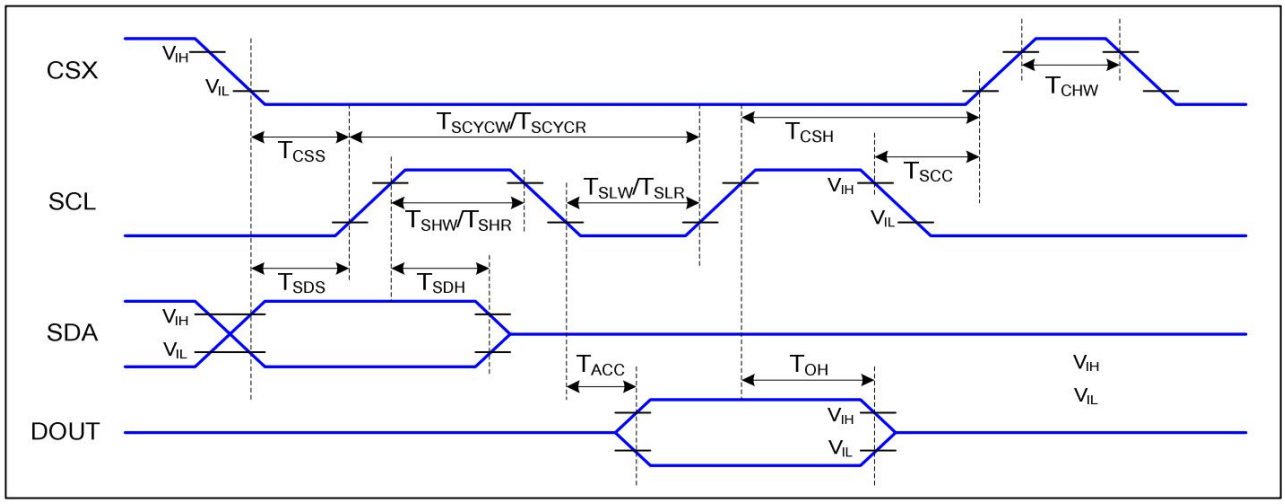
If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until "Power On Sequence" powers it up.

5.3.4 Power Flow Chart



5.4 Timing Characteristics

5.4.1 AC Characteristics

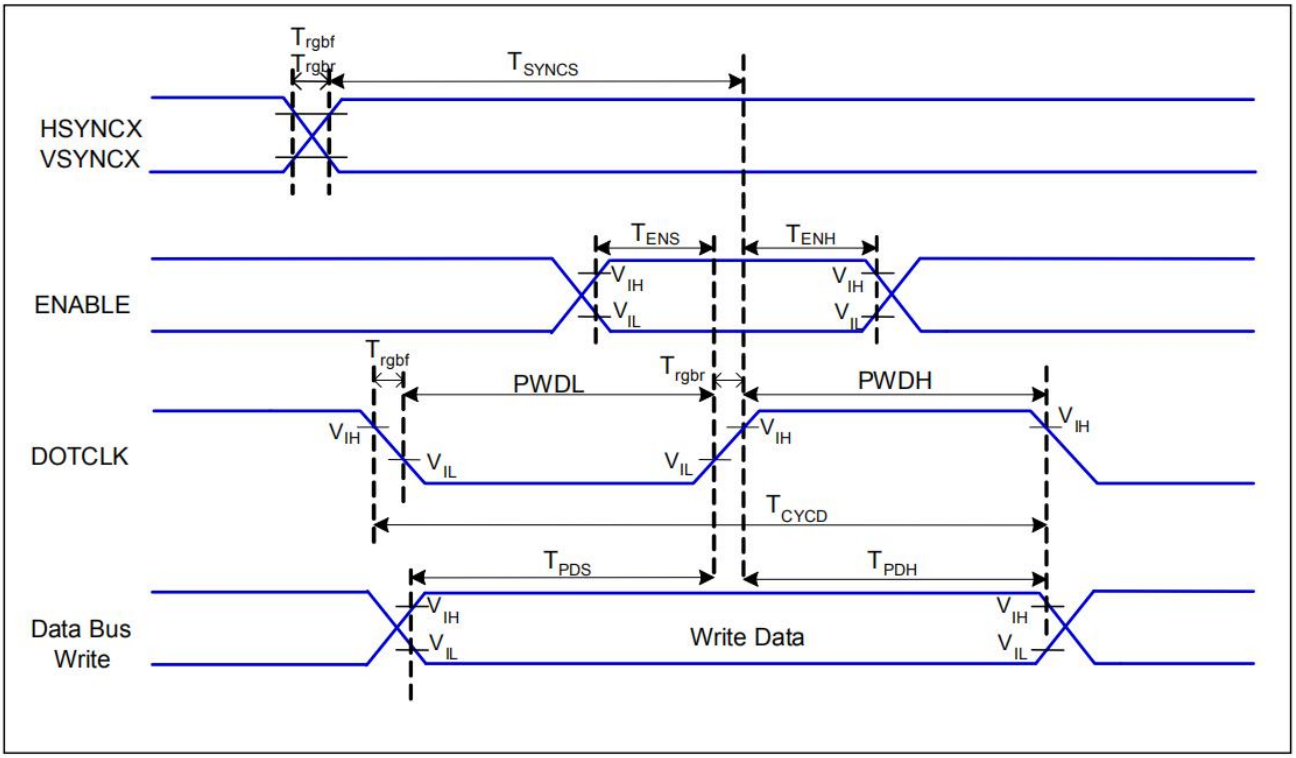


3-SPI Interface Timing Characteristics

VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL “H” pulse width (Write)	15		ns	
	T_{SLW}	SCL “L” pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

3-SPI Interface Characteristics

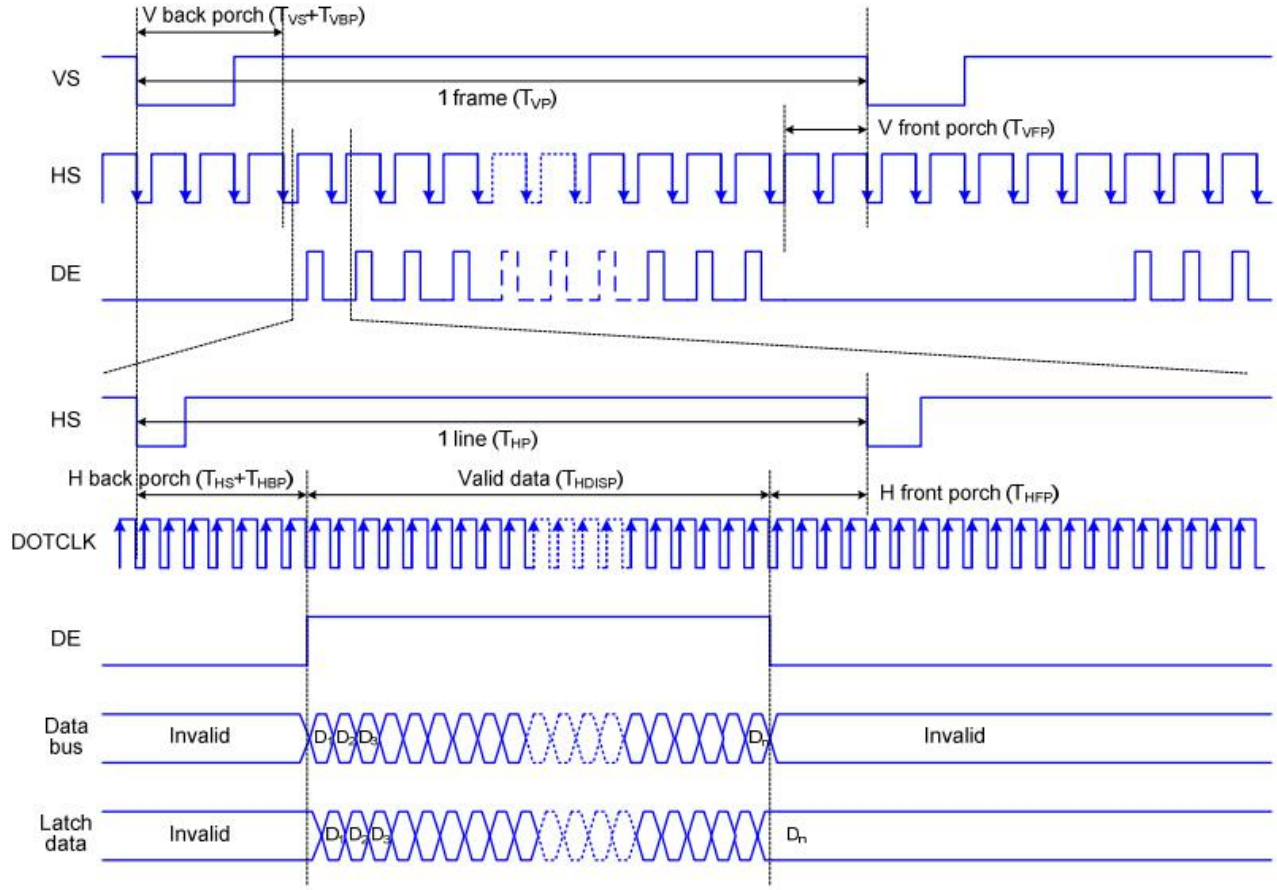


VDDI=1.8V,VDDA=2.8V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	15	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	15	-	ns	
	T_{ENH}	Enable Hold Time	15	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	30	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	30	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	66	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	15	-	ns	
	T_{PDH}	PD Data Hold Time	15	-	ns	

RGB Interface Timing Characteristics

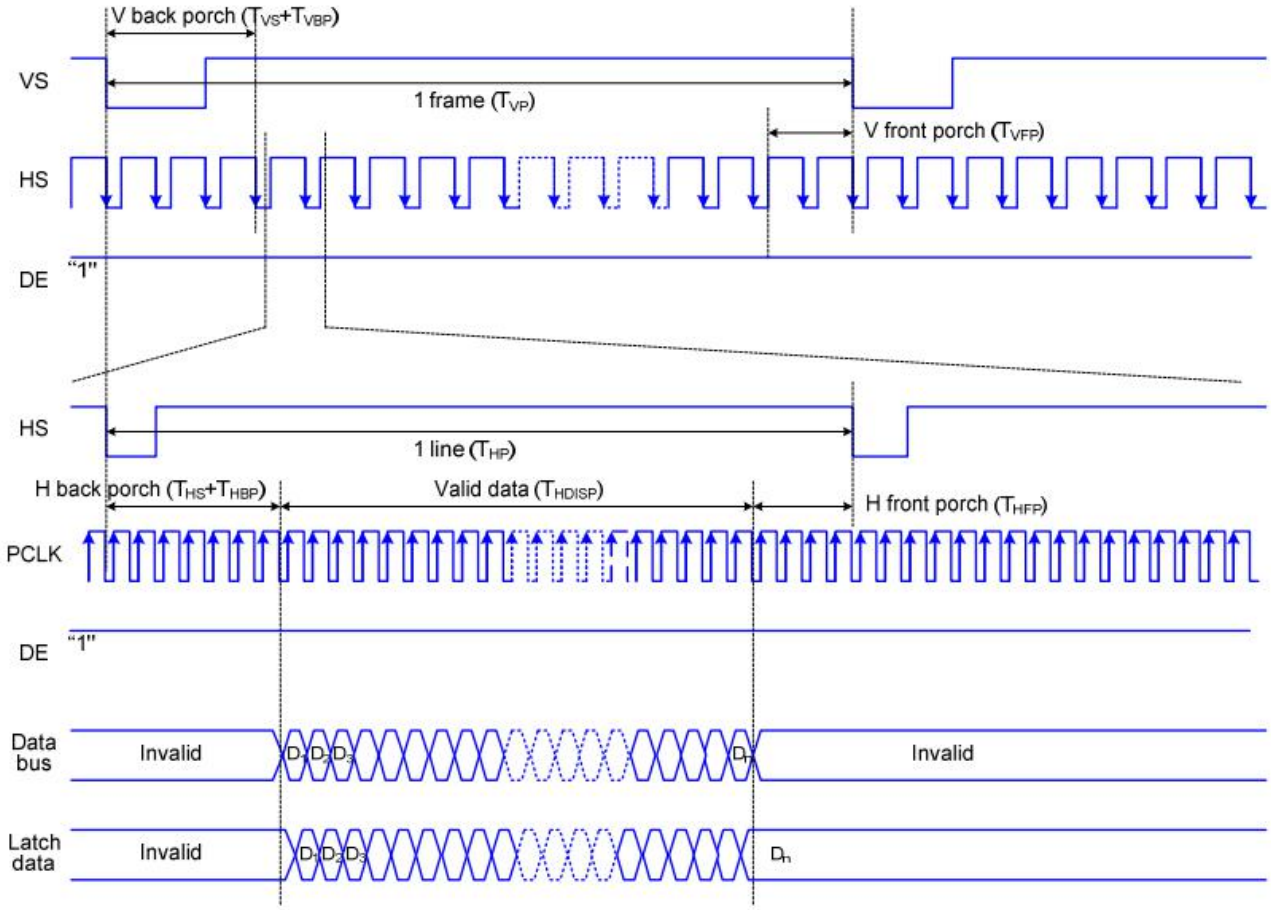
The timing chart of RGB interface DE mode is shown as follows.



Note: The setting of front porch and back porch in host must match that in IC as this mode.

Timing Chart of Signals in RGB Interface DE Mode

The timing chart of RGB interface HV mode is shown as follows.



Timing chart of RGB interface HV mode

The following are the functions not available in RGB Input Interface mode.

Function	RGB Interface	I80 System Interface
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation function	Not available	Available

VSYNC, HSYNC, and DOTCLK signals must be supplied during a display operation period. In RGB interface mode, the panel controlling signals are generated from DOTCLK, not the internal clock generated from the internal oscillator.

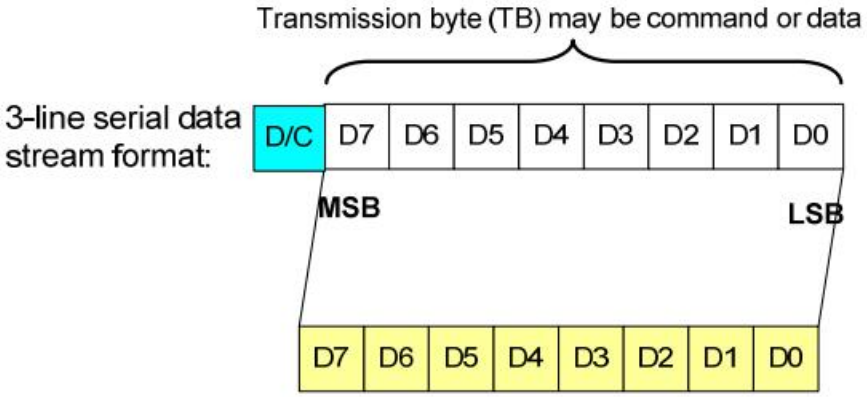
When switching between the internal operation mode and the external display interface operation mode, follow the sequences below in setting instruction.

In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.

In RGB interface mode, a RAM address is set in the address counter every frame on the falling edge of VSYNC.

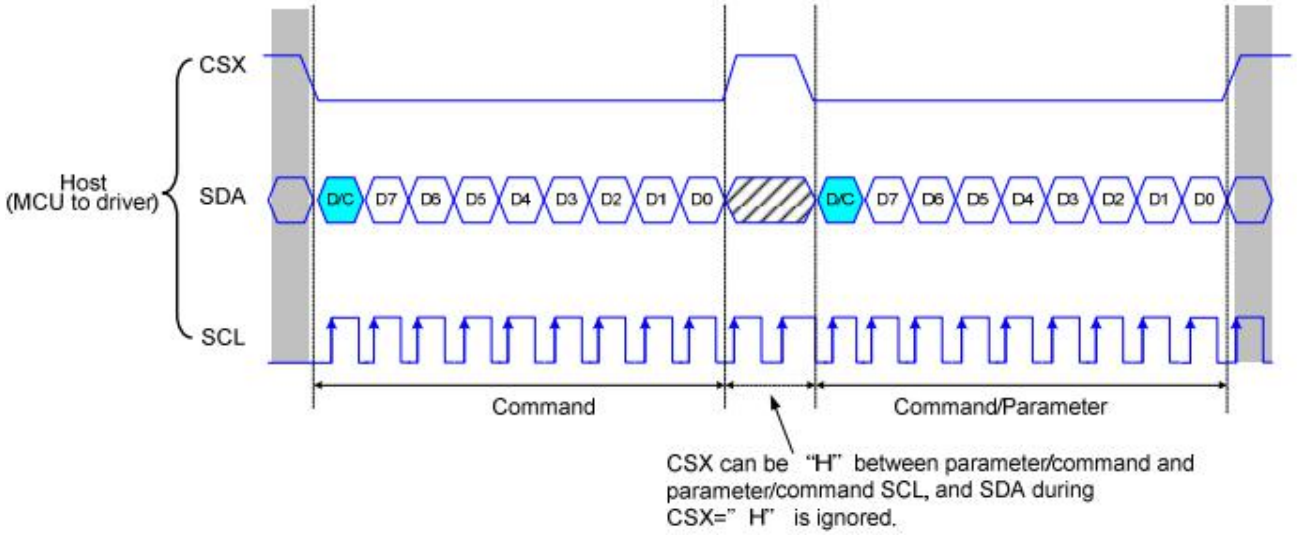
Write Sequence

In the write mode of 3-line serial interface contains a D/CX (data/command) select bit and a transmission byte. If the D/C bit is “0”, the transmission byte is interpreted as a command byte. If the D/C bit is “1”, the transmission byte is display data, or stored in the command register as parameter data.



8 Bit Data Trasmission Byte

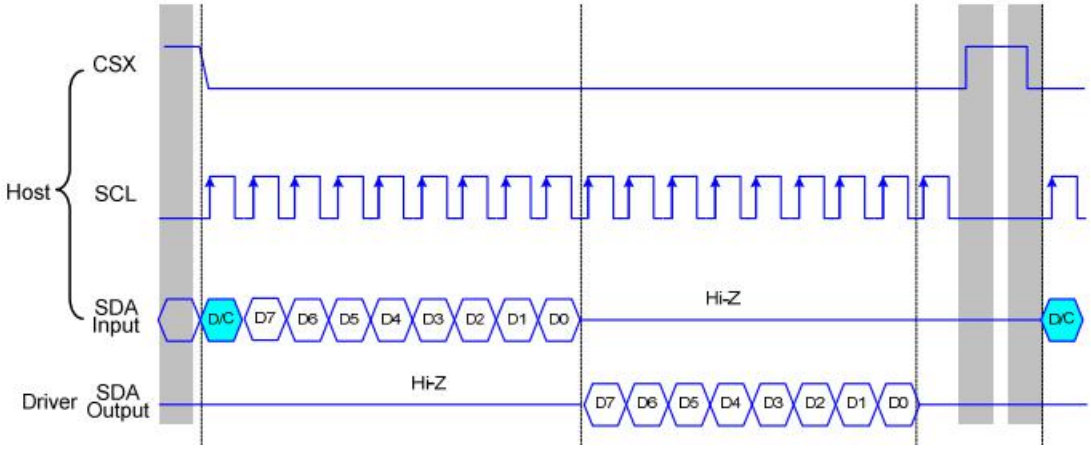
The instruction of ST7796s can be sent in any order, and the MSB is transmitted first. The 3-line serial interface is initialized when the CSX keeps high level. In this state, the SCL clock pulse and SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.



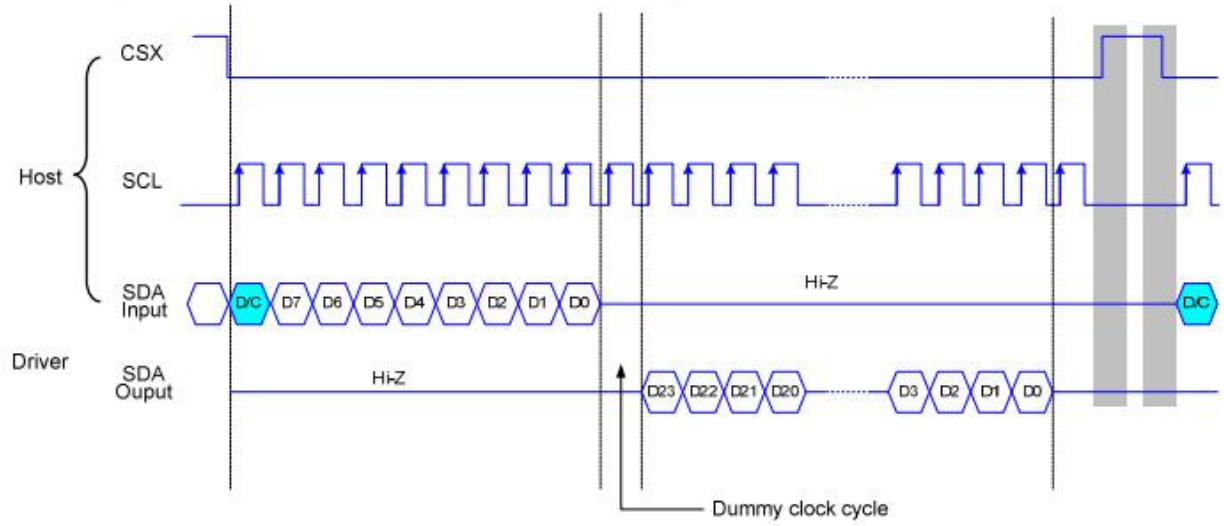
Read Sequence

In the read mode of the interface, the host reads the register value from the ST7796s. The host sends out a command (Read ID or register command), then a byte is (bytes are) transmitted in the opposite direction. The ST7796s samples the SDA (input data) at the rising edges of the SCL (serial clock), and shifts to SDO (output data) at the falling edges of the SCL (serial clock). The read mode has three types of transmitted command data (8-/24-/32-bit) according to the command code.

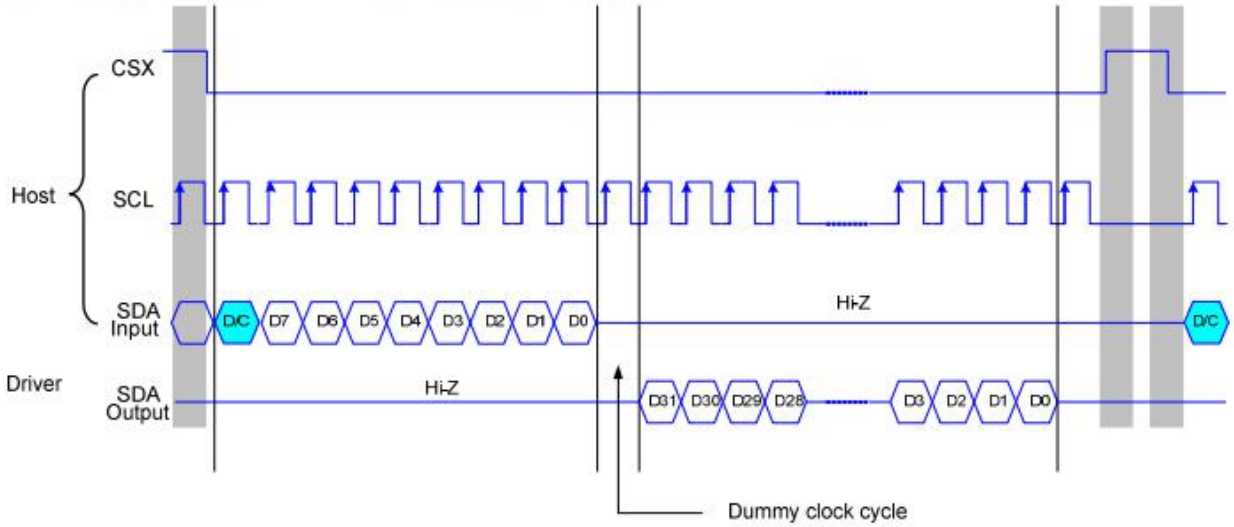
3-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



3-line serial protocol (for RDDID command: 24-bit read)

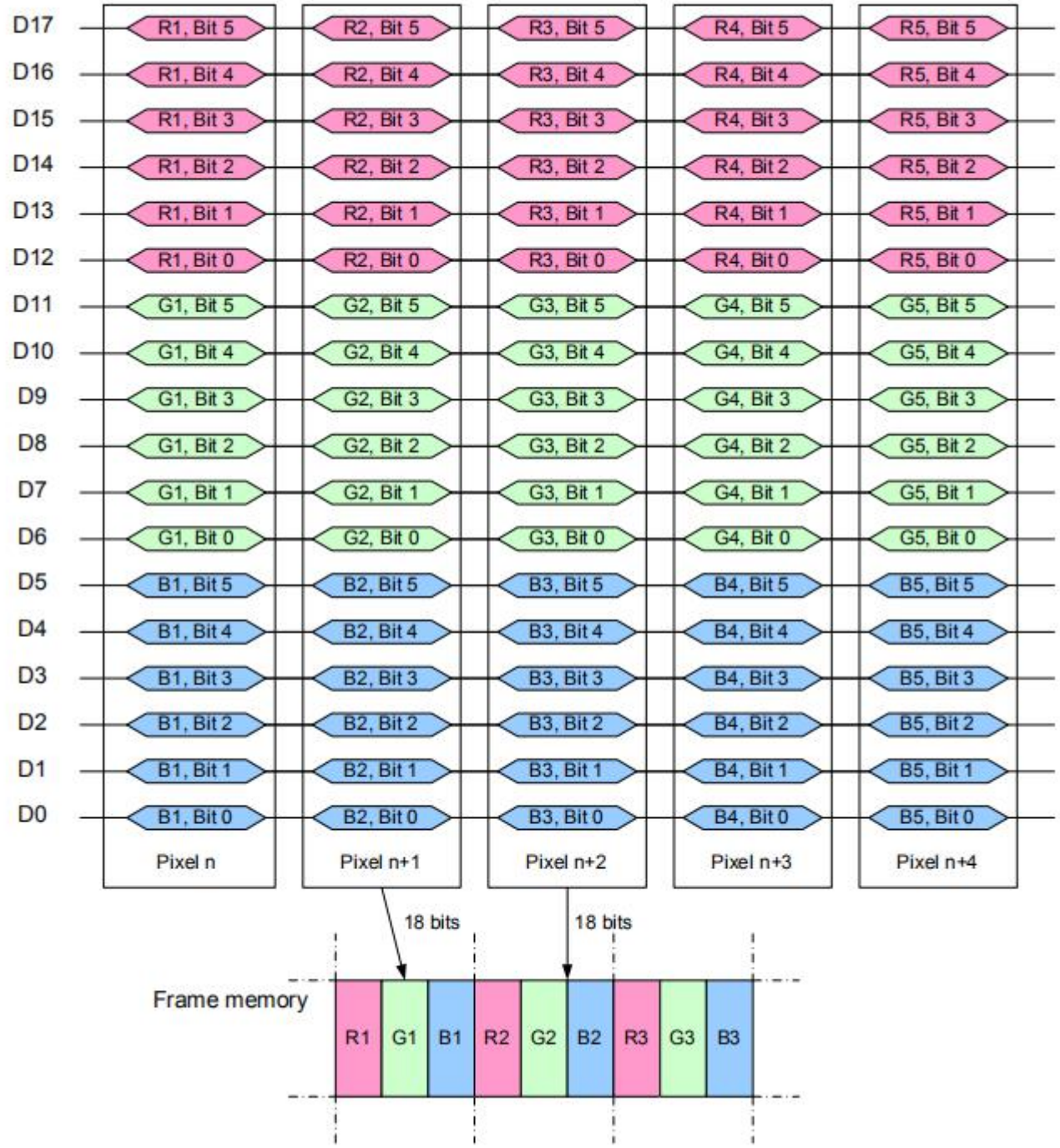


3-line serial protocol (for RDDST command: 32-bit read)

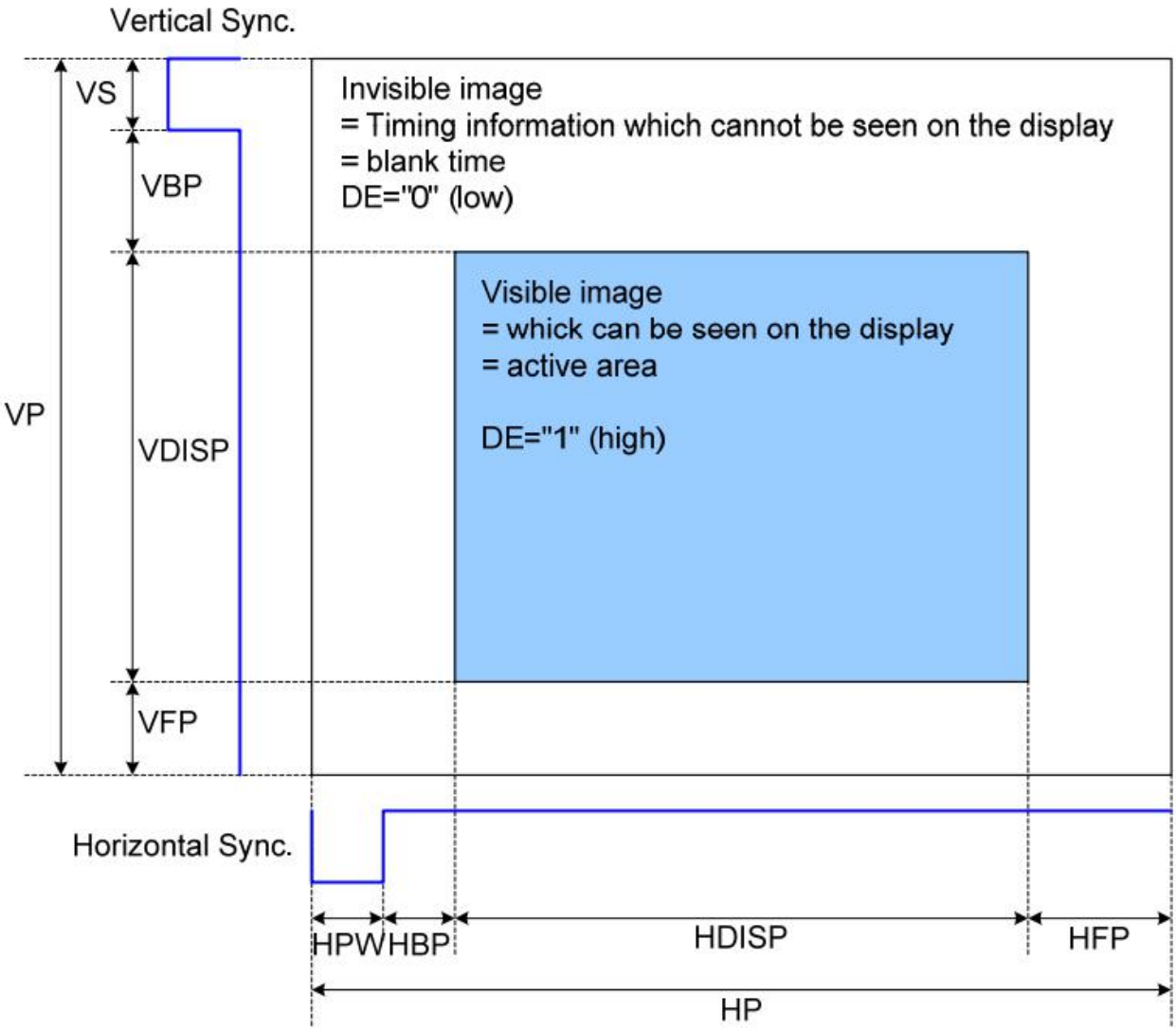


5.4.2 Data Fomat

Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors



The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.



DRAM Access Area by RGB Interface

Please refer to the following table for the setting limitation of RGB interface signals.

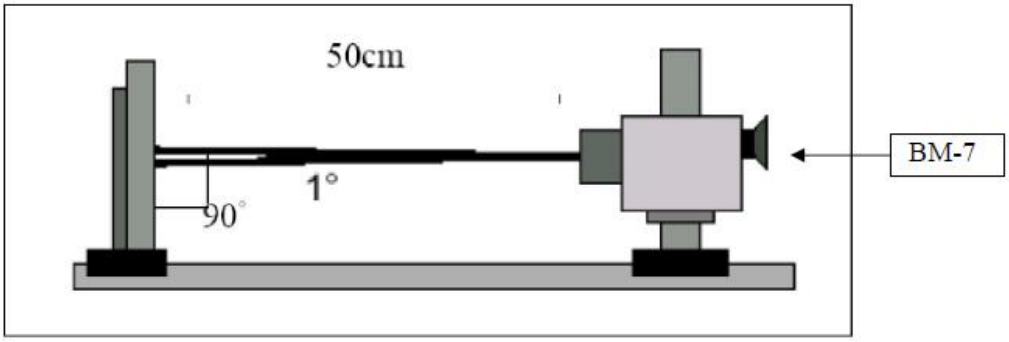
Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	40	50	256	Clock
Horizontal Sync. Back Porch	hbp	40	50		Clock
Horizontal Sync. Front Porch	hfp	2	38	-	Clock
Vertical Sync. Width	vs	2	4	-	Line
Vertical Sync. Back Porch	vbp	2	4		Line
Vertical Sync. Front Porch	vfp	2	8	-	Line

Note:

6. OPTICAL CHARACTERISTICS

Parameter 参数	Symbol 符号	Condition 条件	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Contrast Ratio	C/R	θ = 0°	800	1000	-	-	Note(3)
NTSC Ratio	S	θ =0°	67	72	-	%	Note(10)
Luminance uniformity	U_W	θ =0°	80	-	-	%	Note(7)
Response Time	T_R+ T_F	25 °C	-	-	35	ms	Note(4)
Color Coordination	W_X	θ = 0° (Center) Normal viewing angle B/L On	-0.04	0.311	+0.04	NTSC (x,y)	Note(8)
	W_Y			0.345			
	R_X			TBD			
	R_Y			TBD			
	G_X			TBD			
	G_y			TBD			
	B_X			TBD			
	B_Y			TBD			
Viewing Angle	θ_L	C/R>10		80	-	Degree	Note(5)
	θ_R			80	-		
	θ_U			80	-		
	θ_D			80	-		

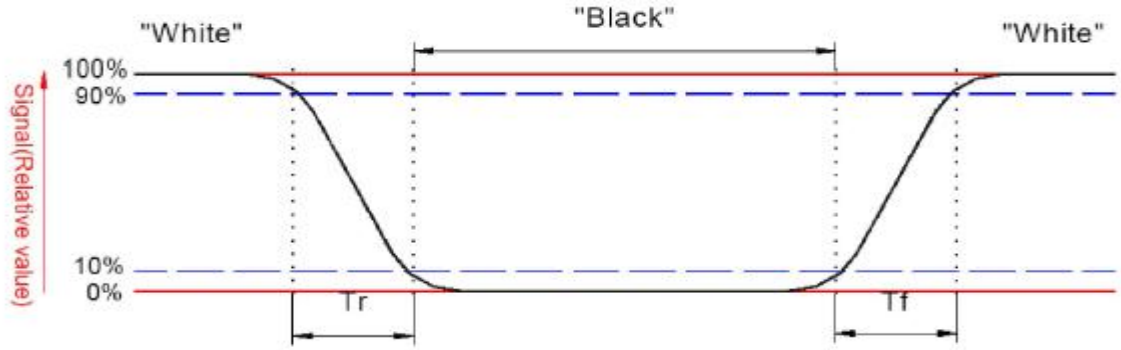
Note 1: Ambient temperature = 25 ± 2 ℃;
Note 2: To be measured in the dark room;
Note 3: To be measured at the center area of the panel with a view cone of 1° by BM-7, after 10 minutes operation (module).



FLG1

Note 4: Define the response time:

The output signals of photo detector are measured when the input signals are charged from "black" to "white"(falling time) and from "white" to "black"(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



FLG2

Note 5: Contrast Ratio (CR) is defined mathematically as For more information from FLG3

Contrast Ratio= Average surface luminance with all white pixel (P1,P2,P3,P4,P5,P6,P7,P8,P9) / Average surface luminance with all black pixel (P1,P2,P3,P4,P5,P6,P7,P8,P9)

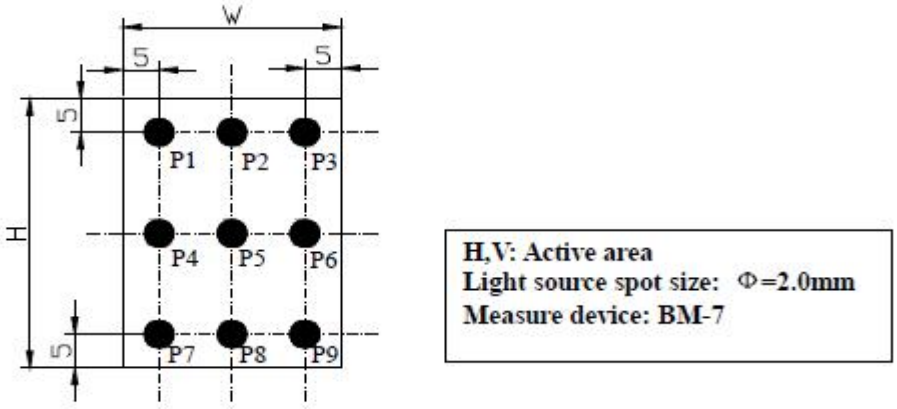
Note 6: Surface luminance is the center point across the LCD surface 500mm from the surface with all pixel displaying white, For more information see the FLG3

Lv= Average Surface luminance with all white pixel(P1,P2,P3,P4,P5,P6,P7,P8,P9)

Note 7: The uniformity in surface luminance, δ white is determined by measuring luminance at each test position 1to 5, and then dividing the maximum luminance of 5 points luminance by minimum luminance of 5 points luminance. For more information see FLG3.

δ WHITE= Minimum surface luminance with all white pixel(P1,P2,P3,P4,P5,P6,P7,P8,P9) / Maximum surface luminance with all white pixel(P1,P2,P3,P4,P5,P6,P7,P8,P9)

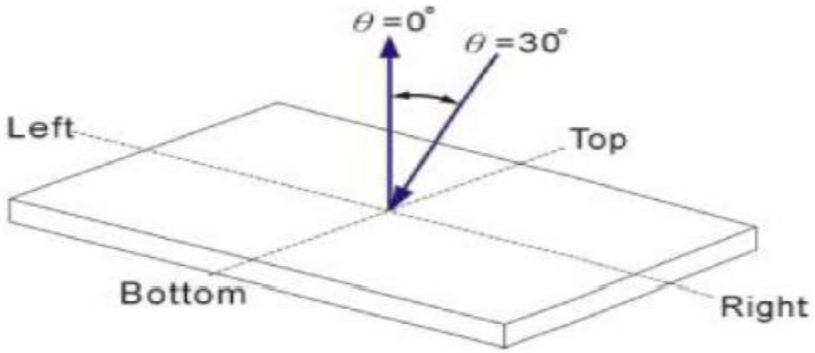
Note 8: CIE(X, Y), the X, Y value is determined by measuring luminance at each test position 1 to 5, and then make average value. For more information see FLG3.



FLG3

Note 9: Viewing angle is the angle at which the contrast ratio is greater than 2, TFT module the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the

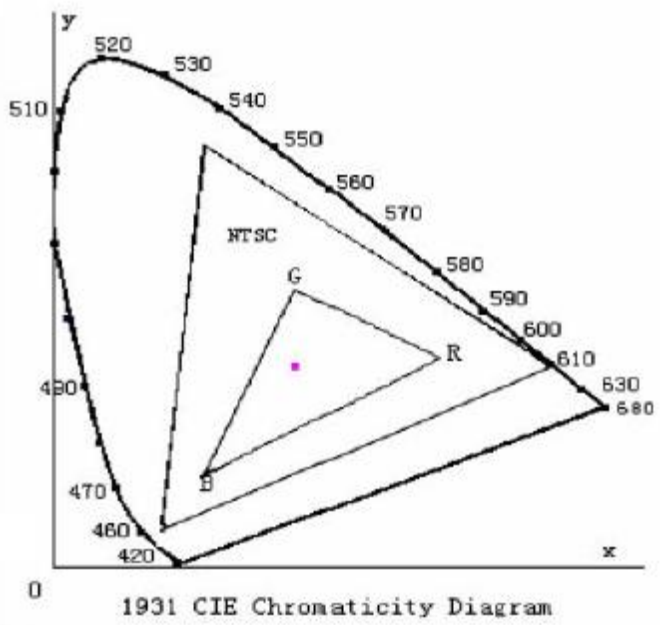
vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see the FLG 4.



FLG4

Note 10: Definition of NTSC ratio:

$$\text{NTSC ratio} = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}}$$



1931 CIE Chromaticity Diagram

7. RELIABILITY

Item 项目	Test Condition 测试条件	Remark 备注
High Temperature Storage	Ta =+80°C / 96Hours	Note1,2,3
Low Temperature Storage	Ta =-30°C / 96Hours	Note1,2,3
High Temperature Operating	Ta =+70°C / 96Hours	Note1,2,3
Low Temperature Operating	Ta =-20°C / 96Hours	Note1,2,3
Temperature Cycle storage Test	-30°C/30min ⇆+80°C /30min for 30cycles,Transfer time less than 5min	Note2,3
Thermal humidity storage Test	60°C x 90%RH / 96Hours	Note2,3
Package Vibration Test	Frequency: 10Hz~55Hz,Amplitude:1.5mm, 1 hrs for each direction of X, Y, Z	Note2

Inspection after Test:

Note1:Ta is the ambient temperature of samples.

Note 2: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but doesn't guarantee all the cosmetic specification.

Note 3: Before cosmetic and function tests , the product must have enough recovery time, at least 2 hours at room temperature.

Note 4: In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

8. PACKAGE DRAWING