LCD MODULE

SPECIFICATION

Model:	LCM-UEED055HD-RB40-L004A
Version:	V1.0
Date:	2023 07 26

Customer Confirmation 客户确认

Approved by	Notes

Please return one of the copies of the specification with your signature to us within two weeks after you receive this document. If it is not returned, we will assume that you agree to the entire contents of this specification document.

请贵司在收到规格书的两周内，将签好字的规格书原件或者复印件寄回.如果没有返回，我司将会认为贵司已经默认接受产品规格书中的全部资料和规范.

VIEWE Confirmation 优奕确认

Prepared by	Reviewed by	Approved by

REVISION HISTORY

Revision 版本号	Date 日期	Contents of Revision Change 修改内容	Remark 备注
V1.0	2023 07 26	Preliminary release	

TABLE of CONTENTS

1. GENERAL INFORMATION

1.1 Features

1) Pixel Arrangement：RGB Vertical Stripe
2) Interface Mode：MIPI 4 Lane
3) Driver IC：ST7703
4) Operation Temperature：-30~80℃
5) Storage Temperature：-35~85℃
6) Backlight Type：White LED
7) Display mode：Transflective Normally BLACK
8) LED life time：30,000 Hours

1.2 Mechanical Specification

Item 项目	Specification 规格	Unit 单位	Remark 备注
Pixel Driving element	TFT	-	-
Screen Size	5.5	Inch	Diagonal
Resolution	720(H)*3(RGB)*1440(V)	Dots	-
Interface	MIPI	-	4 Lane
Module Power Consumption	0.146	Watt	Reflective Mode
	0.986		Transmissive Mode
Luminance	8.5%*Surrounding illumination	cd/m²	Reflective Mode
	100+8.5%*Surrounding illumination	cd/m²	Transmissive Mode
Active Area	120.96(W)*60.48(H)	mm	-
Pixel pitch (W*H)	0.084(W)*0.084(H)	mm	-
Module Size (W*H*D)	130.51(W)*64.24(H)*1.64(D)	mm	Typ
Display Color	16.7M	Colors	

Applicate Suggestion:

Backlight off in Reflective mode @ Surrounding illumination > 1500 cd/m²

Backlight on in Transmissive mode @ Surrounding illumination ≤ 1500 cd/m²

Please contact Viewe for Surrounding illumination (lx) detail information

2. ABSOLUTE MAXIMUM RATINGS

Item 项目	Symbol 符号	Min. 最小值	Max. 最大值	Unit 单位	Remark 备注
Power supply1 voltage	VDD	-0.3	6.6	V	Note1
LED Reverse Voltage	V_R	-	5	V	For each led,Note1
Operating temperature	T_{op}	-30	80	°C	Note1,2
Storage temperature	T_{st}	-35	85	°C	Note1,2
Humidity	H_{st}	10	90	%RH	Note1,3

(Ta=+25°C,GND=0V)

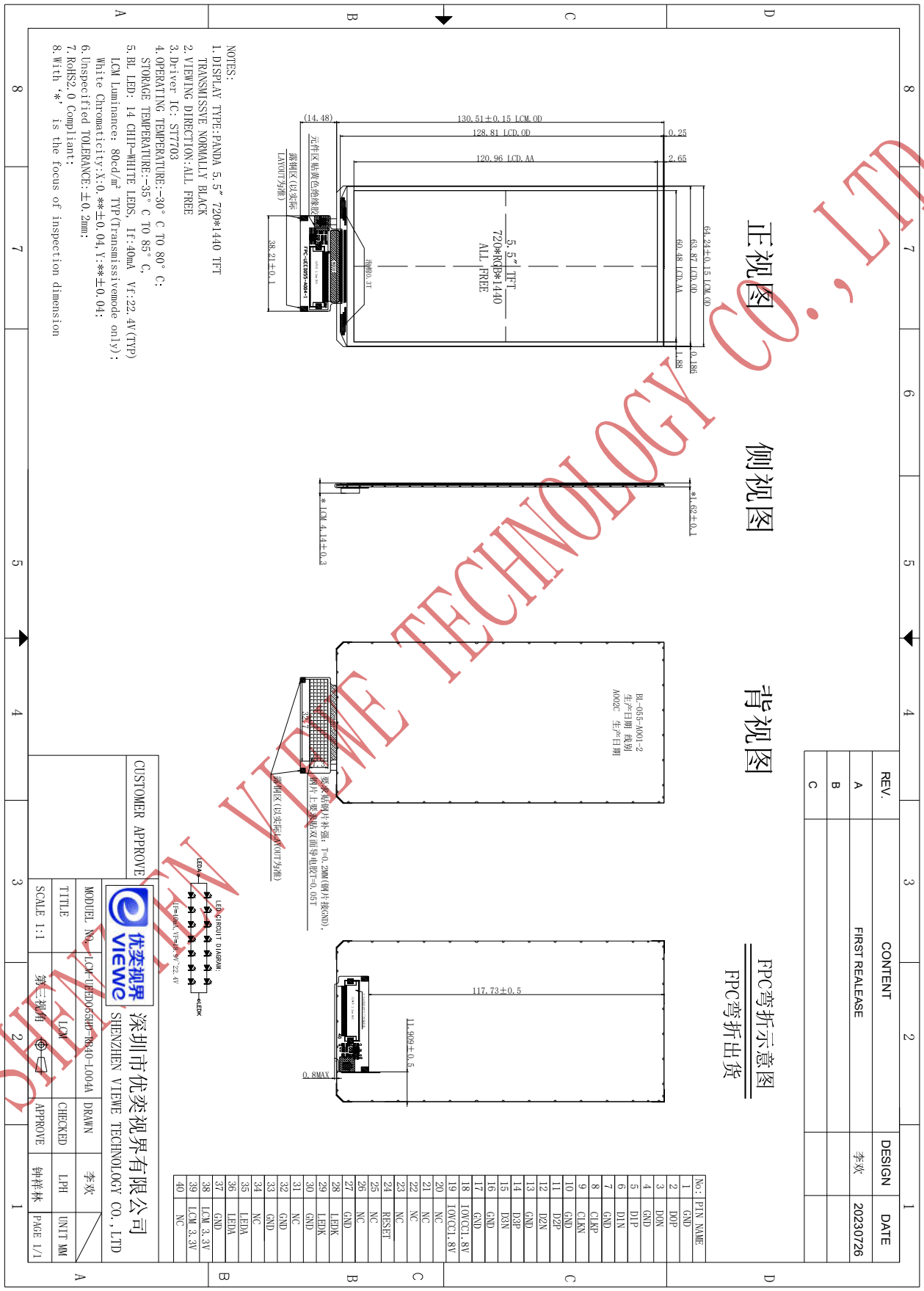
Note1:If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also if the module operates with the absolute maximum ratings for a long time, the reliability may drop.

Note2: In case of temperature below 0℃,the response time of liquid crystal (LC) becomes slower and the color of panel darker than normal one.

Note3: Temp. ≤ 60℃ , 90% RH MAX.

Temp. ＞60℃ , Absolute humidity shall be less than 90% RH at 60℃.

3. MECHANICAL DRAWING



No.	PIN NAME
1	GND
2	DOP
3	DON
4	GND
5	D1P
6	D1N
7	GND
8	CLKP
9	CLKN
10	GND
11	D2P
12	D2N
13	GND
14	D3P
15	D3N
16	GND
17	GND
18	IOVCC1.8V
19	IOVCC1.8V
20	NC
21	NC
22	NC
23	NC
24	RESET
25	NC
26	NC
27	GND
28	LEDK
29	LEDK
30	GND
31	NC
32	GND
33	GND
34	NC
35	LEDA
36	LEDA
37	GND
38	LCM_3.3V
39	LCM_3.3V
40	NC

4. I/O CONNECTION & BLOCK DIAGRAM

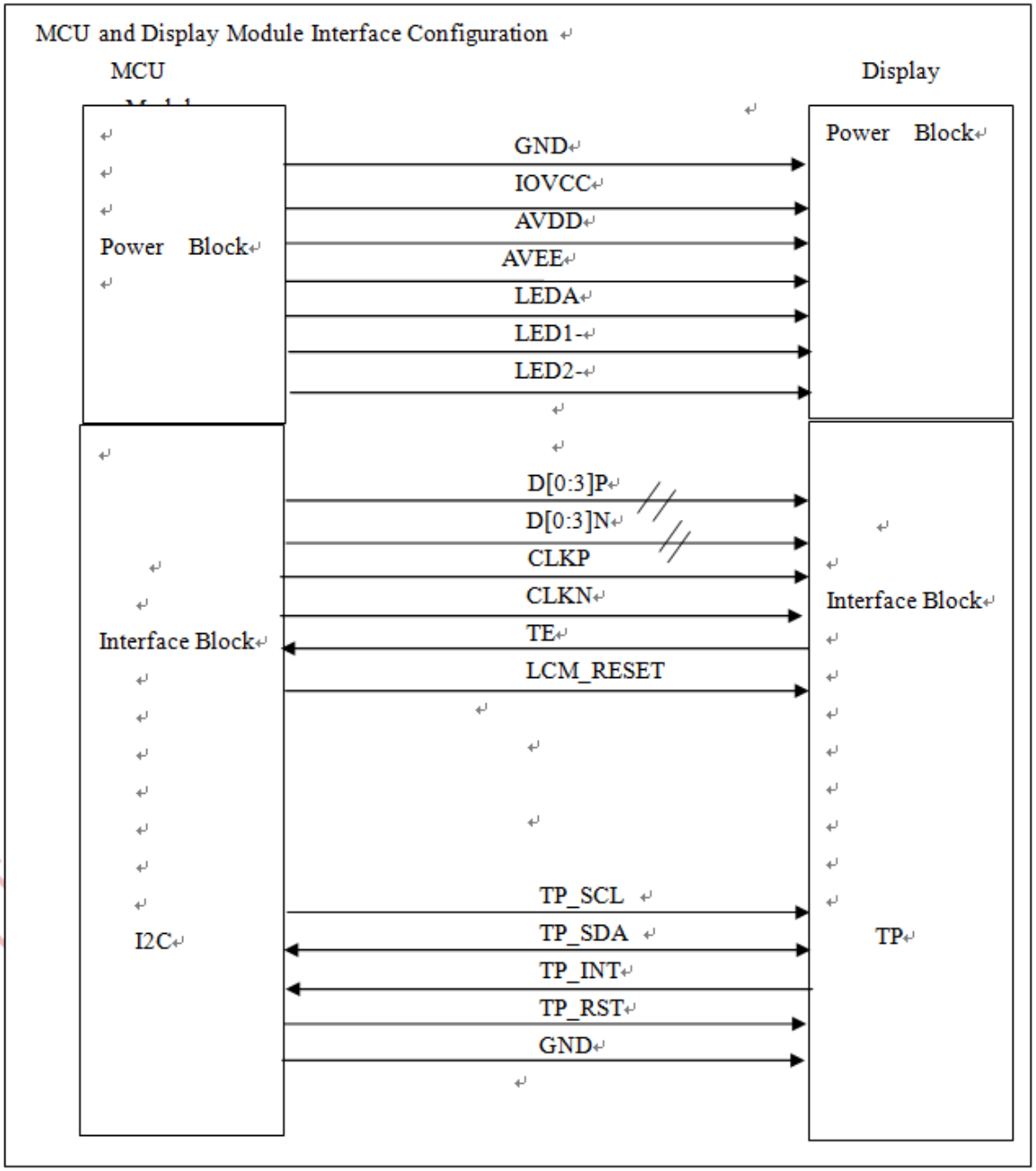
4.1 I/O Connection

Pin No. 序号	Symbol 符号	I/O	Description 描述
1	GND	P	Power Ground
2	D0P	I/O	MIPI-DSI data lane 0 positive-end input pin
3	D0N	I/O	MIPI-DSI data lane 0 negative-end input pin
4	GND	P	Power Ground
5	D1P	I	MIPI-DSI data lane 1 positive-end input pin
6	D1N	I	MIPI-DSI data lane 1 negative-end input pin
7	GND	P	Power Ground
8	CLKP	I	MIPI-DSI data clock lane positive-end input pin
9	CLKN	I	MIPI-DSI data clock lane negative-end input pin
10	GND	P	Power Ground
11	D2P	I	MIPI-DSI data lane 2 positive-end input pin
12	D2N	I	MIPI-DSI data lane 2 negative-end input pin
13	GND	P	Power Ground
14	D3P	I	MIPI-DSI data lane 3 positive-end input pin
15	D3N	I	MIPI-DSI data lane 3 negative-end input pin
16-17	GND	P	Power Ground
18-19	IOVCC 1.8	P	Power supply for logic circuits and IO pads(1.8V)
20-23	NC	-	No connected
24	RESET	I	The signal will reset the LCM, Signal is active low.
25-26	NC	-	No connected
27	GND	P	Power Ground
28-29	LEDK	P	Power supply for backlight cathode
30	GND	P	Power Ground
31	NC	-	No connected
32-33	GND	P	Power Ground
34	NC	-	No connected
35-36	LEDA	P	Power supply for backlight anode
37	GND	P	Power Ground
38-39	LCM-3.3V	P	Positive input analog power for driver IC use
40	NC	-	No connected

I：Input；O：Output；P：Power

4.2 Block Diagram

MCU and Display Module Interface Configuration



5. ELECTRICAL CHARACTERISTICS

5.1 TFT-LCD Panel Driving Section

Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Power Supply1 Voltage	IOVCC	1.65	1.8	2	V	-
Power Supply2 Voltage	AVDD	4.5	5.8	6	V	
Power Supply3 Voltage	AVEE	-6	-5.8	-4.5	V	
Power Supply1 Current	I_{VCI}		16.5		mA	
Power Supply2 Current	I_{AVDD}		10.5		mA	
Power Supply3 Current	I_{AVEE}		9.7		mA	
Logic Input High Voltage	V_{IH}	0.7IOVCC	-	IOVCC	V	-
Logic Input Low Voltage	V_{IL}	VSSD	-	0.3IOVCC	V	-

(Ta=+25°C,GND=0V)

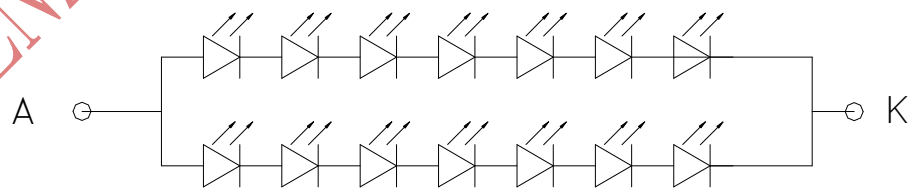
Note1:Measurement Conditions : Full Screen Red Pattern,IOVCC=1.8V,60Hz Refresh.

5.2 Back Light Driving Section

Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Forward Voltage	V_F	-	21	-	V	Note1
Forward Current	I_F	-	40	-	mA	Note1
Backlight Power consumption	P_{BL}	-	0.84	-	Watt	Note1
LED life time	-	30000	-	-	Hours	Note2
LED Quantity			14		PCS	

(Ta=+25°C,GND=0V)

Note1:The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_{LED}=20mA(Per Led). The LED life time could be decreased if operating I_{LED} is larger than 20mA.



5.3 Power On/Off Sequence

Power source IOVCC, VCI can be applied and powered down in any order. IOVCC, VCI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, IOVCC, VCI must be powered down minimum 120msec after NRESET has been released.

During power off, if LCD is in the Sleep In mode, IOVCC, VCI can be powered down minimum 0msec after NRESET has been released.

NCS can be applied at any timing or can be permanently grounded. NRESET has priority over NCS.

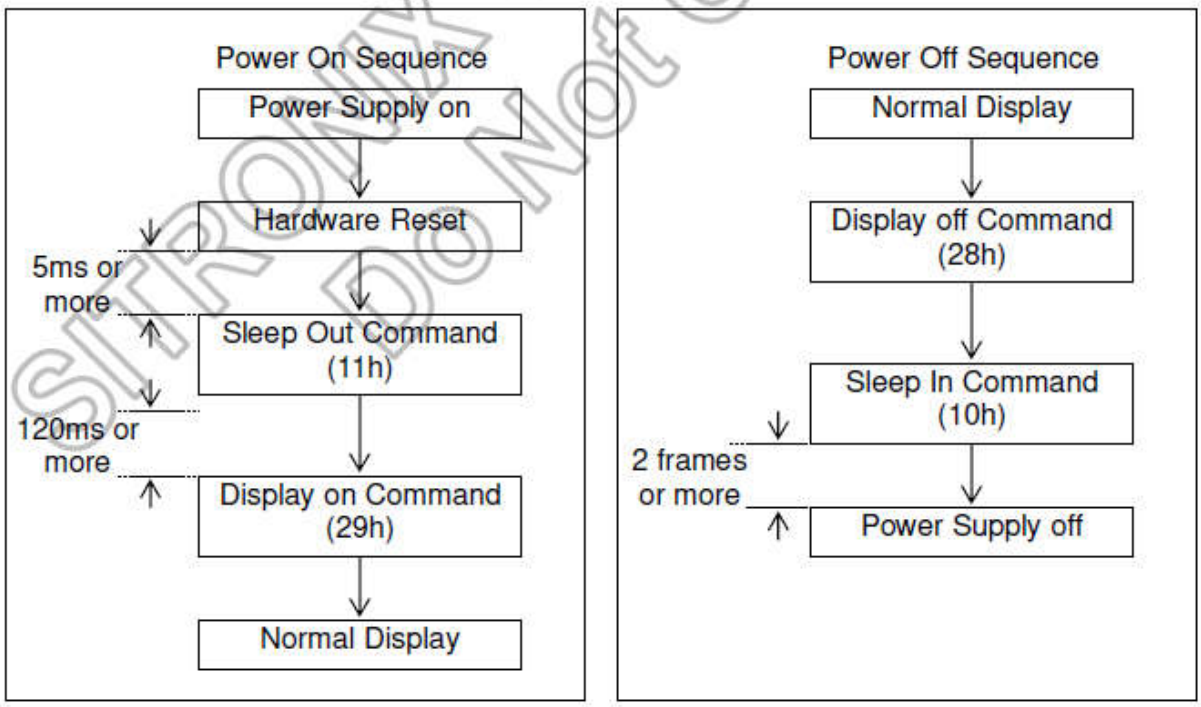


Figure 5.32: The power supply ON/OFF setting for Display ON/OFF and Sleep In/out

5.3.1 Case 1: RESX line is held high or unstable by host at power on

If RESX line is held high or unstable by the host during power on, then a Hardware Reset must be applied after both VDD1, VDD2 and VDD3 have been applied- otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

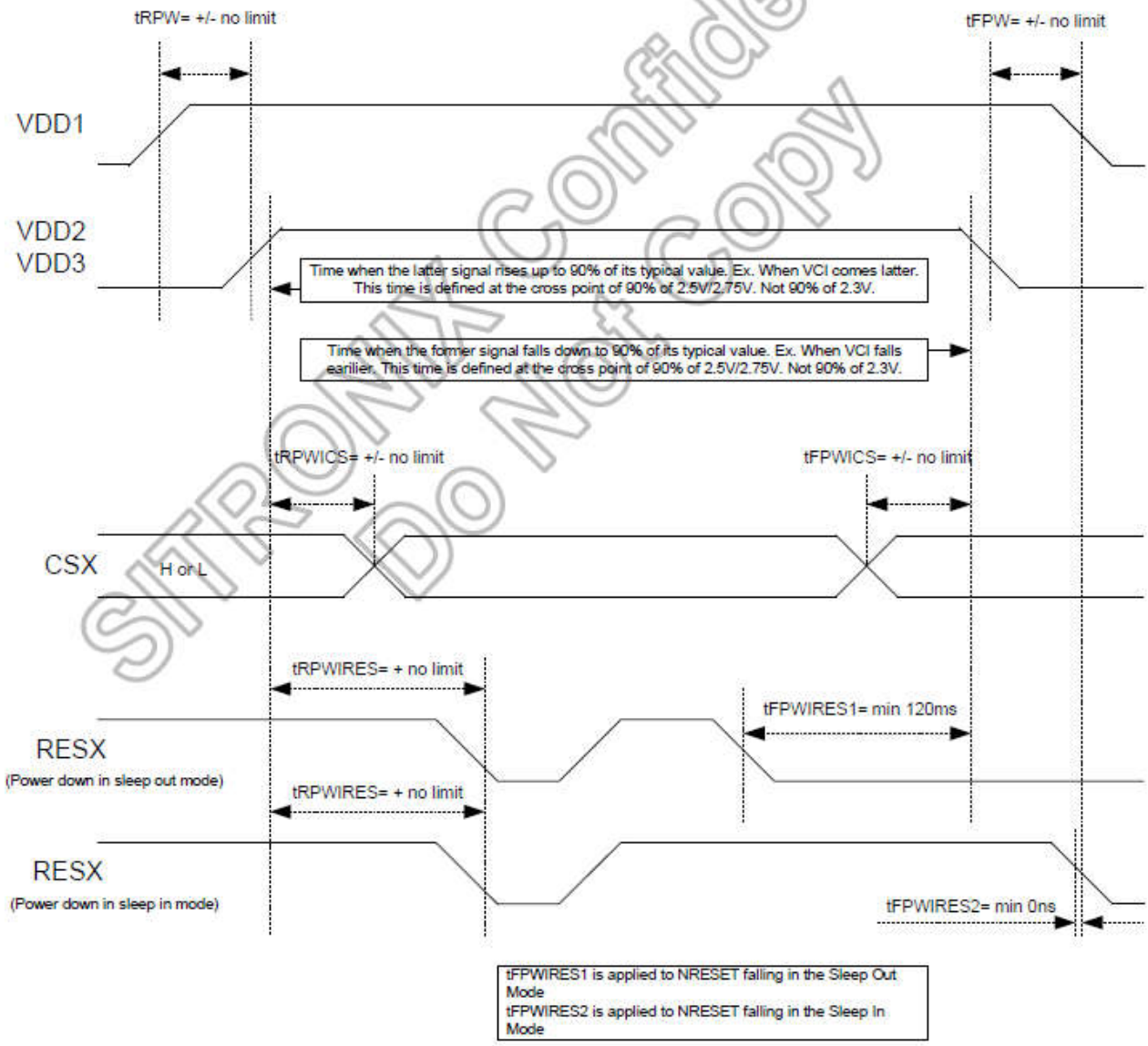
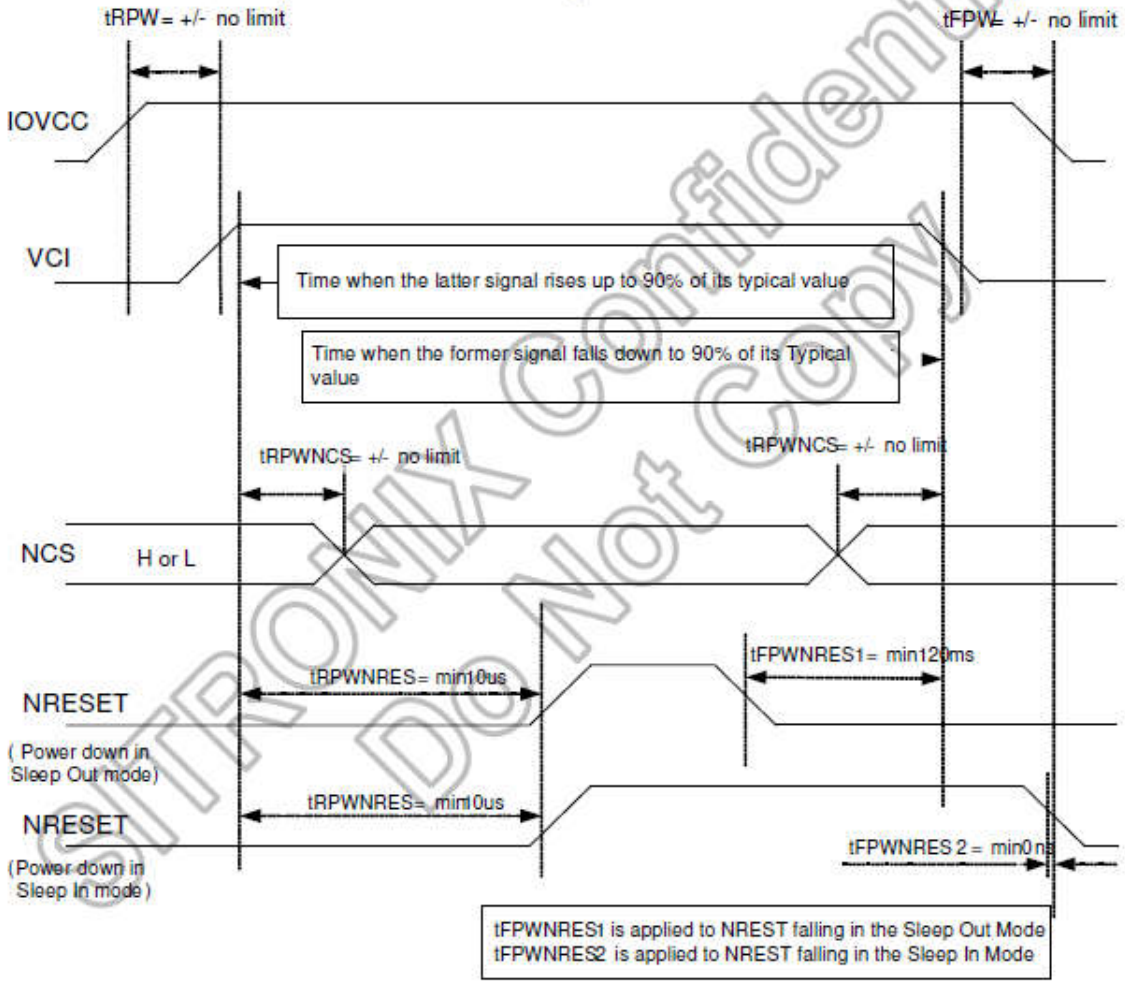


Figure 5.33: Case 1: RESX line is held high or unstable by host at power on

5.3.2 Case 2: RESX line is held low by host at power on

If RESX line is held low (and stable) by the host during power on, then the RESX must be held low for minimum 10µsec after both VDD1, VDD2 and VDD3 have been applied.



Note: Unless otherwise specified timings herein show cross point at 50% of signal/power level

Figure 5.34: Case 2: RESX line is held low by host at power on

5.4 AC Characteristics

High Speed Mode

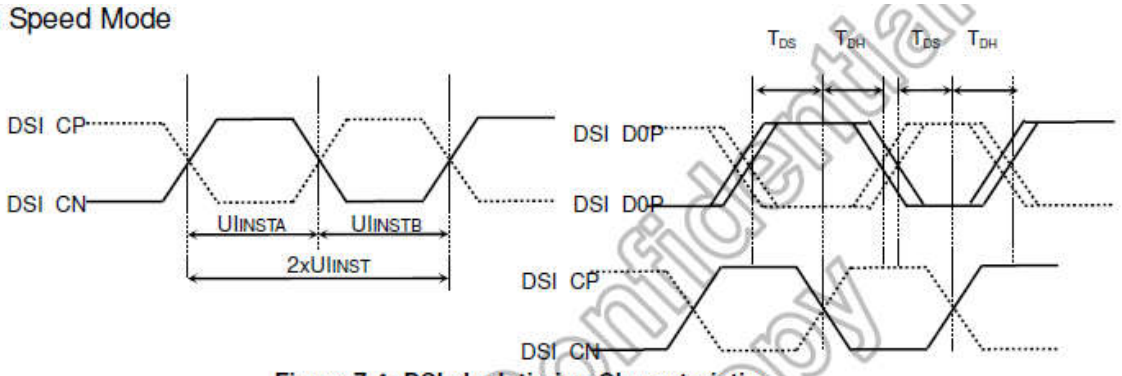


Figure 7.4: DSI clock timing Characteristics

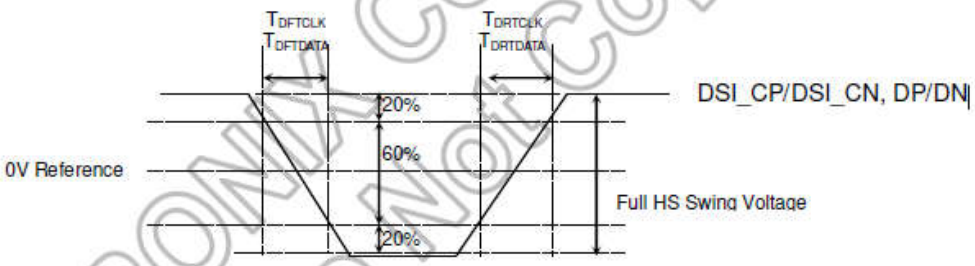


Figure 7.5: Rising and falling time on clock and data channel

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	2xUINST	TBD	-	25	ns
	UI instantaneous	UINSTA UINSTB	TBD	-	12.5	ns
DP/DN	Data to clock setup time	TDS	0.15xUI	-	-	ps
	Data to clock hold time	TDH	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	TDRTCLK	150	-	0.3UI	ps
	Differential fall time for clock	TDFTCLK	150	-	0.3UI	ps
DP/DN	Differential rise time for data	TDRTDATA	150	-	0.3UI	ps
	Differential fall time for data	TDFTDATA	150	-	0.3UI	ps

Table 7.3: DSI High Speed Mode Characteristics

Low Power Mode

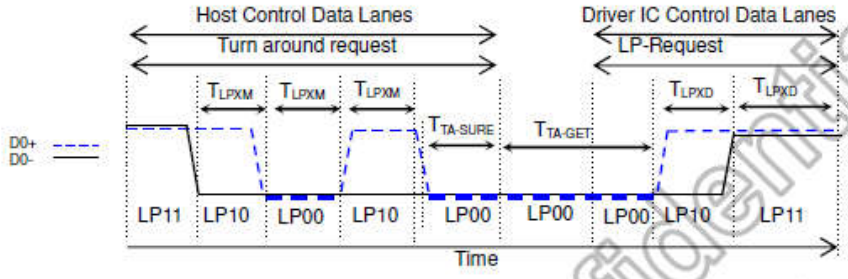


Figure 7.6: BTA from HOST to Display Module Timing

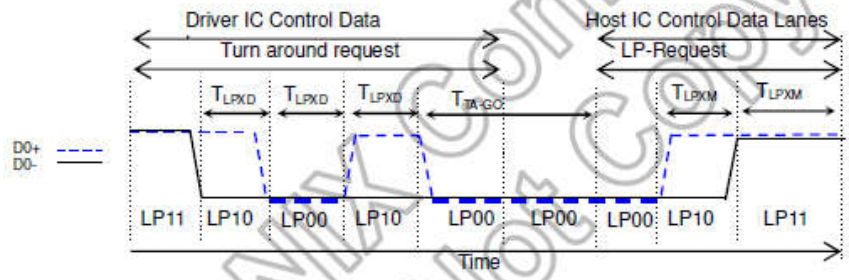


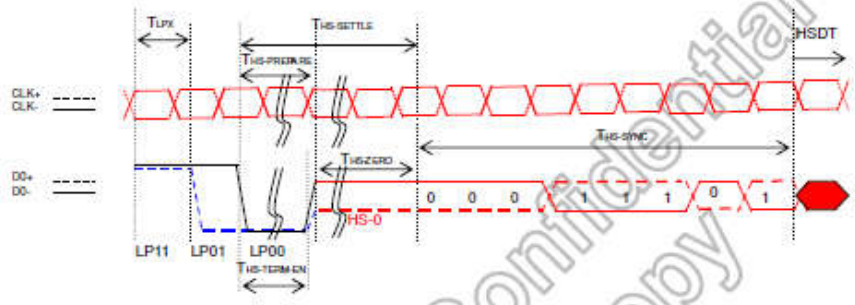
Figure 7.7: BTA from Display Module Timing to HOST

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host→ Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module →Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	2xT_{LPXD}	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

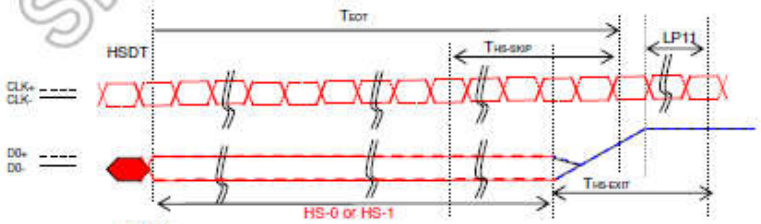
Table 7.4: DSI Low Power Mode Characteristics

DSI BURSTS



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	TLPX	50	-	-	ns
	Time to Driver LP-00 to prepare for HS transmission	THS-PREPARE	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	THS-TERM-EN	-	-	35+4xUI	ns
	Time to drive LP-00 by display module	TTA-GET	5xTLPXD	-	-	ns
	Time to drive LP-00 after turnaround request Host	TTAGO	4xTLPXD	-	-	ns

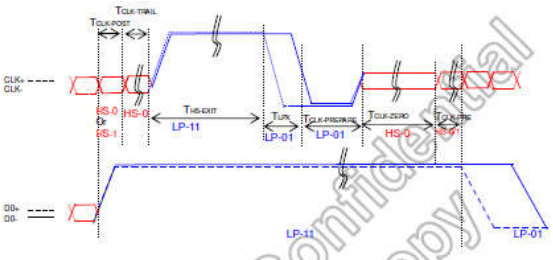
Table 7.5: DSI Low Power Mode to High Speed Mode Timing



NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	THS-SKIP	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	THS-EXIT	100	-	-	ns

Table 7.6: DSI Low Power Mode to High Speed Mode Timing



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	TCLK-POST	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	TCLK-TRAIL	60	-	-	ns
	Time to drive LP-11 after HS burst	THS-EXIT	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	TCLK-PREPARE	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	TCLK-TERM-EN	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	TCLK-PREPARE + TCLK-ZERO	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	TCLK-PRE	8xUI			

Table 7.7: Clock Lanes High Speed Mode to/from Low Power Mode Timing

5.5 DSI Power On/Off Timing

5.5.1 Power On Timing of External Power IC

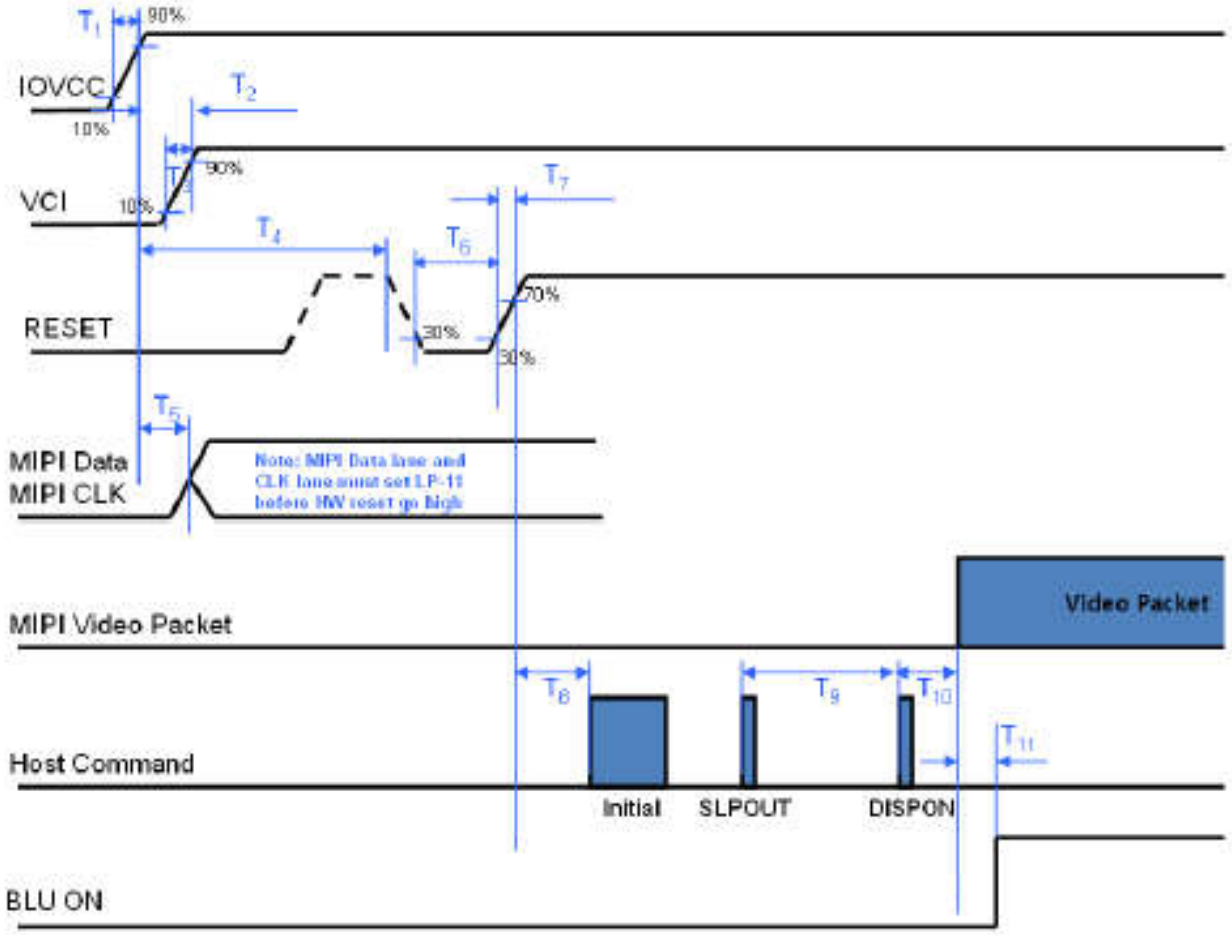


Figure 8-6: DSI Power On Sequence of Power IC Mode

	Min.	Typ.	Max.	Unit
T1	0.01	-	10	ms
T2		No Limit		ms
T3	0.01	-	10	ms
T4	1	-	-	ms
T5	1	-	-	ms
T6	10	-	-	us
T7		No Limit		ns
T8	15	-	-	ms
T9	120	-	-	ms
T10		No Limit		ms
T11	100	150	-	ms

Table 8-1: DSI Power On Timing of Power IC Mode

5.5.2 Power off Timing of External Power IC

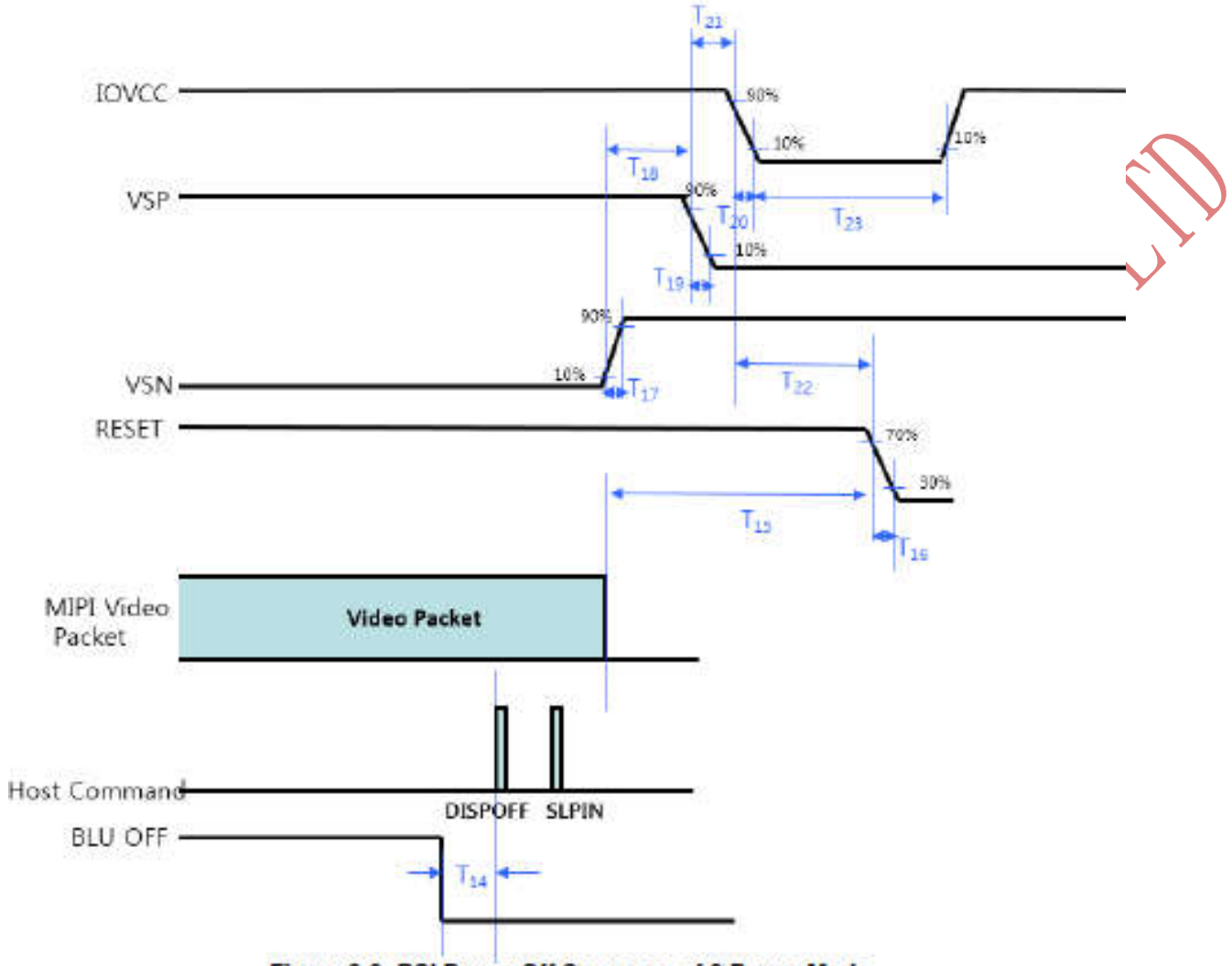


Figure 8-9: DSI Power Off Sequence of 3 Power Mode

	Min.	Typ.	Max.	Unit
T14	40	100	-	ms
T15	10	-	-	ms
T16	No Limit			ms
T17	No Limit			ms
T18	1	-	-	ms
T19	No Limit			ms
T20	No Limit			ms
T21	1	-	-	ms
T22	1	-	-	ms
T23	100	-	-	ms

Table 8-4: DSI Power Off Timing of 3 Power Mode

5.5.3 Timing Parameters

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Vertical low pulse width	VS	-	-	4	-	Line
Vertical front porch	VFP	-	-	32	-	Line
Vertical back porch	VBP	-	-	16	-	Line
Vertical active area	VDISP	-	-	720	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz
HS low pulse width	HS	-	-	20	-	DCK
Horizontal back porch	HBP	-	-	40	-	DCK
Horizontal front porch	HFP	-	-	60	-	DCK
Horizontal active area	HDISP	-	-	1440	-	DCK

6. OPTICAL CHARACTERISTICS

6.1 Optical Specification (Reflective mode)

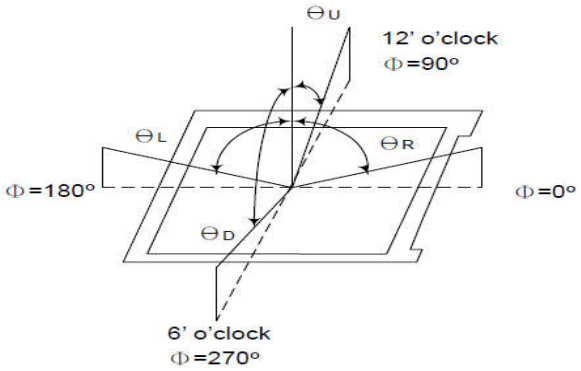
Parameter 参数	Symbol 符号	Condition 条件	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
White Reflectance (with Polarizer)	Rw (%)	θ = 0		8.5		%	
Contrast Ratio	C/R	θ = 0°	-	15:1	-	-	
NTSC Ratio	S	θ =0°	-	14	-	%	
Response Time	T_R+ T_F	25 °C	-	-	30	ms	设备：DMS Tr+Tf W90%/B10%
Viewing Angle	θ L	C/R>2	-	55	-	Degree	设备：DMS Source pad Down CR>2
	θ R		-	55	-		
	θ U		-	55	-		
	θ D		-	55	-		

6.2 Optical Specification (Transmittance mode)

Parameter 参数	Symbol 符号	Condition 条件	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Contrast Ratio	C/R	θ = 0°		45:1	-	-	SR-UL1R
NTSC Ratio	S	θ =0°		18		%	
Luminance	L	θ =0°		100	-	cd/m2	
Luminance uniformity	U_W	θ =0°	80	-	-	%	Note(1)
Response Time	T_R+ T_F	25 °C	-	-	30	ms	Note(2)
Color Coordination	W_X	θ =0°	-+0.04	-	+0.04	NTSC (x,y)	Note(3)
	W_Y			-			
Viewing Angle	θ L	C/R>2	-	60	-	Degree	设备：DMS source pad down CR>2
	θ R			60			
	θ U			60			
	θ D			60			

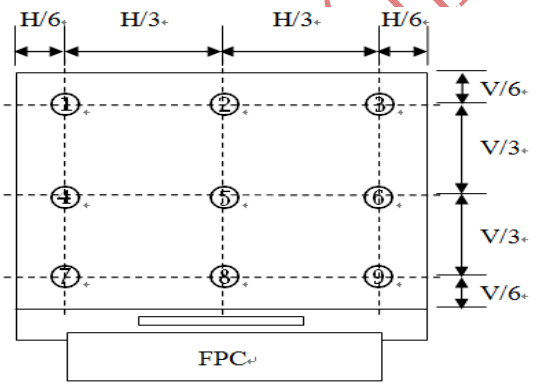
Test Conditions:
1. the ambient temperature is+25℃.
2. The test systems refer to Note 8.

Definition of Viewing Angle: The viewing angle range that the CR>2

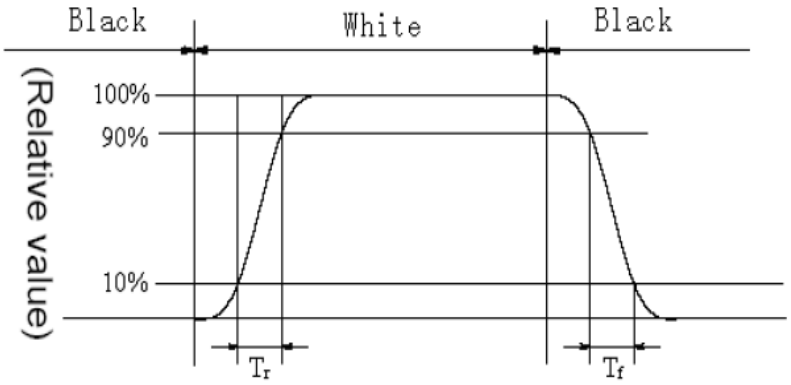


Note 1: Definition of Luminance Uniformity: Active area is divided into 9 measuring areas, every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity} = \frac{\text{Min Luminance of white among 9-points}}{\text{Max Luminance of white among 9-points}} \times 100\%$$



Note2: Definition of Response time: Sum of T_R and T_F

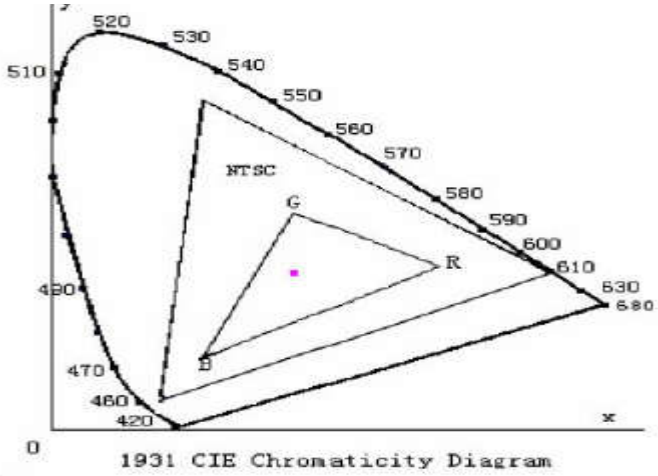


Note 3:
Definition of Color Chromaticity (CIE 1931)

Color coordinates of white & red, green, blue measured at center point of LCD.

Note 7: Definition of NTSC ratio:

$$\text{NTSC ratio} = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}}$$



7. RELIABILITY

Item 项目	Test Condition 测试条件	Remark 备注
High Temperature Storage	Ta = +85°C / 96Hours	Note1,2,3
Low Temperature Storage	Ta = -35°C / 96Hours	Note1,2,3
High Temperature Operating	Ta = +80°C / 96Hours	Note1,2,3
Low Temperature Operating	Ta = -30°C / 96Hours	Note1,2,3
Temperature Cycle storage Test	-35°C/30min Δ+85°C /30min for 30cycles,Transfer time less than 5min	Note2,3
Thermal humidity storage Test	60°C x 90%RH / 96Hours	Note2,3
Package Vibration Test	Frequency: 10Hz~55Hz,Amplitude:1.5mm, 1 hrs for each direction of X, Y, Z	Note2
Packing shock test	Drop to the ground from 1m height, 1 corner, 3 edges, 6 surfaces.	Note2

Inspection after Test:

Note1:Ta is the ambient temperature of samples.

Note 2: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but doesn't guarantee all the cosmetic specification.

Note 3: Before cosmetic and function tests , the product must have enough recovery time, at least 2 hours at room temperature.

8. PACKAGE DRAWING

第一步

将产品放入吸塑盘中，LCD AA 面朝上，注意防呆方向

第二步

每一层吸塑盘与相邻层，叠放时相错 180 度，最上层不放产品，总叠加层数参考

第三步

检查无误后用胶带固定吸塑盘，将捆好的吸塑盘放入无尘带中并封口；

First step

Putting products into the tray,
LCD A.A faces Upward,
(pay attention to the

Second step

Neighbouring trays should be staggered 180° while stacking up.
on the top,there is an empty tray without product

Third step

Taping up the tray after inspection,and put them into a PE

第四步

外箱内侧底部和四周放上泡棉将包好的产品装入纸箱，合盖；

第五步

最后胶带封箱，贴外箱标签

第六步

将每箱整齐放在栈板上并包裹最高可堆叠 6 层)

Fourth step

Putting EPE foams and products with trays into the carton;
Close the carton box

fifth step

Sealing the carton with cellulose tape ;
Stick on a carton label,

sixth step

Placing the boxes together on a pallet (6 layers at most),