LCD MODULE
SPECIFICATION

Model:	UE030WV-RH40-L003A
Version:	V1.0
Date:	20230426

Customer Confirmation 客户确认

Approved by	Notes

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VIEWE Confirmation 优奕确认

Prepared by	Reviewed by	Approved by

REVISION HISTORY

Revision 版本号	Date 日期	Contents of Revision Change 修改内容	Remark 备注
V1.0	20230426	Preliminary release	

TABLE of CONTENTS

1. GENERAL INFORMATION

1.1 Features

1) Pixel Arrangement：RGB_Stripe
2) Interface Mode： 3SPI +RGB 18BIT
3) Driver IC：GC9503CV；
4) Operation Temperature：-20~70℃
5) Storage Temperature：-30~80℃
6) Backlight Type：White LED
7) Display mode：Normally Black
8) Pixel Density：244 PPI
9) LED life time：30,000 Hours

1.2 Mechanical Specification

Item 项目	Specification 规格	Unit 单位	Remark 备注
Pixel Driving element	IPS TFT	-	
Screen Size	3.0	Inch	Diagonal
Resolution	360(W)*RGB*640(H)	Dots	-
Interface	MIPI	-	2 lanes
Module Power Consumption	0.52	Watt	Typ.
Active Area	36.72(W)*65.28(H)	mm	Typ.
View Area	37.12(W)*65.68(H)	mm	Typ.
Pixel pitch (W*H)	0.102(W)*0.102(H)	mm	Typ.
Module Size (W*H*D)	42.64(W)*74.51(H)*2.35(D)	mm	Typ.
Luminance	310	cd/m^2	Typ.
Viewing Direction	All	O'clock	-
Display Color	262K	Colors	18bit

2. ABSOLUTE MAXIMUM RATINGS

Item 项目	Symbol 符号	Min. 最小值	Max. 最大值	Unit 单位	Remark 备注
Power supply2 voltage	VCI	-0.3	4.6	V	Note1
Power supply3 voltage	IOVCC	-0.3	4.6	V	Note1
Power supply4 voltage	TP_VCI	-0.3	3.6	V	Note1
LED Reverse Voltage	V_R	-	5	V	For each led,Note1
Operating temperature	T_{op}	-20	70	°C	Note1,2
Storage temperature	T_{st}	-30	80	°C	Note1,2
Humidity	H_{st}	10	90	%RH	Note1,3

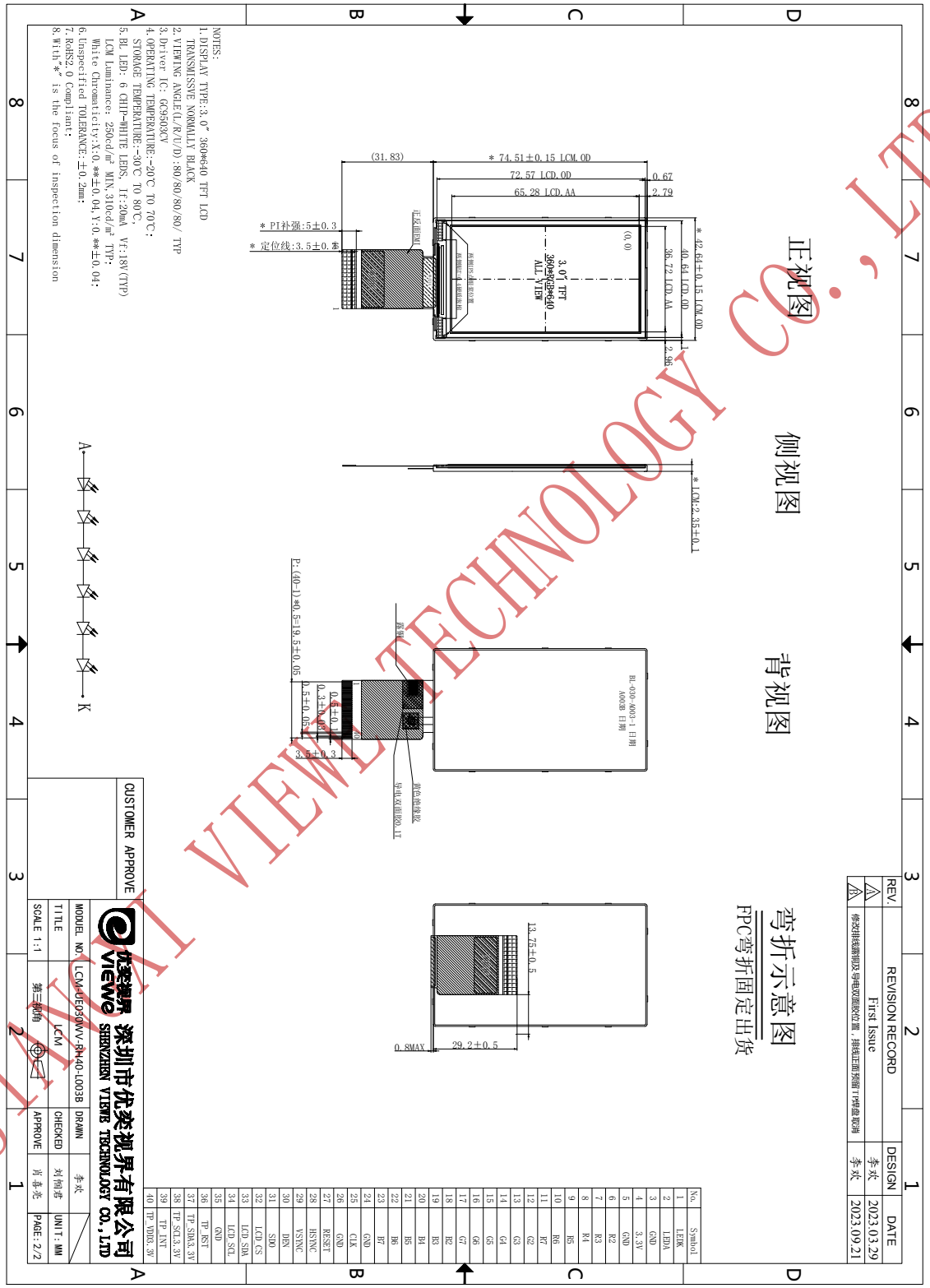
(Ta=+25°C,GND=0V)

Note1:If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also if the module operates with the absolute maximum ratings for a long time, the reliability may drop.

Note2: In case of temperature below 0℃,the response time of liquid crystal (LC) becomes slower and the color of panel darker than normal one.

Note3: Temp. ≤ 60℃ , 90% RH MAX.
Temp. ＞60℃ , Absolute humidity shall be less than 90% RH .

3. MECHANICAL DRAWING



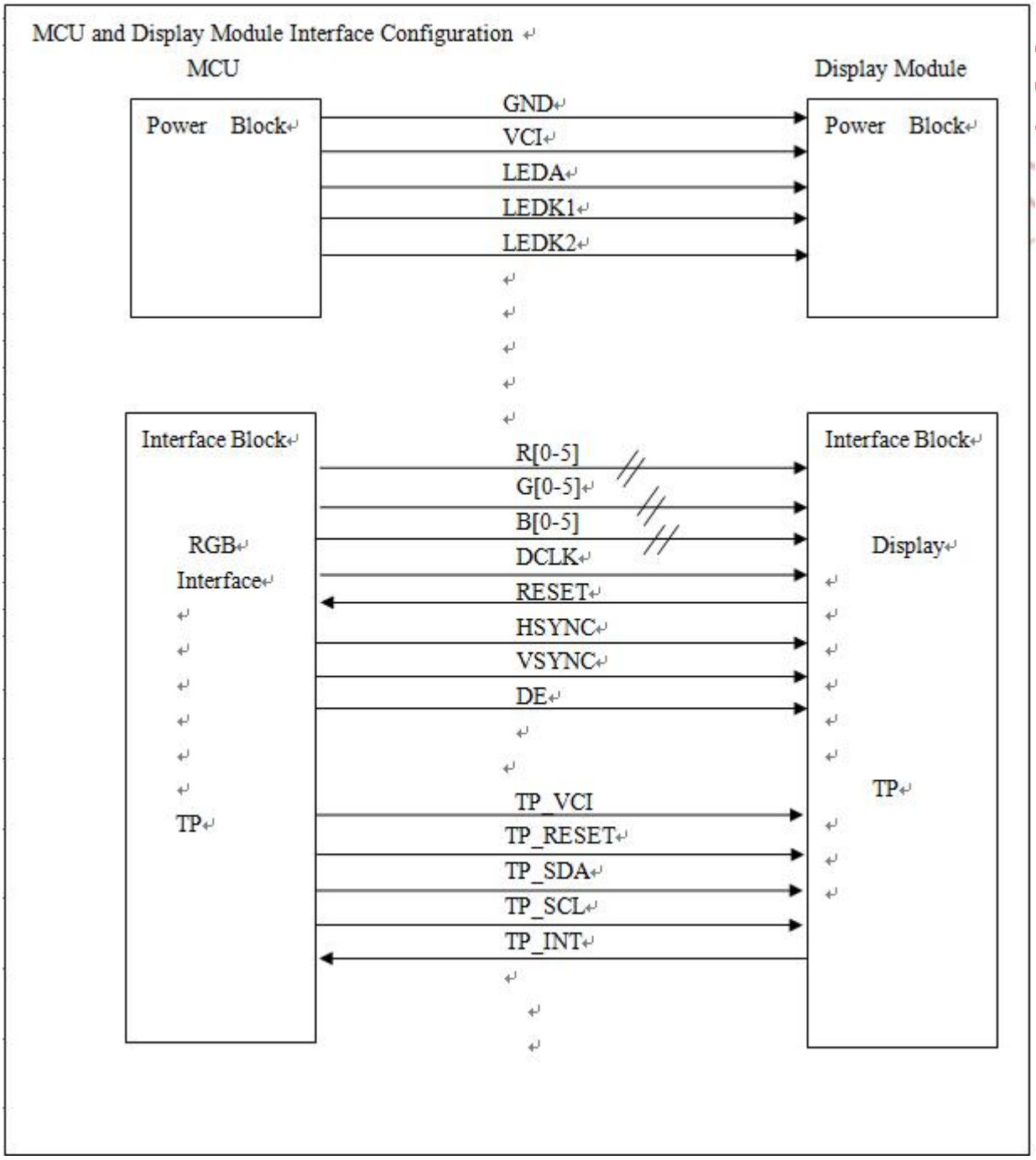
4. I/O CONNECTION & BLOCK DIAGRAM

4.1 I/O Connection

Pin No. 序号	Symbol 符号	I/O	Description 描述
1	LEDK	P	Power supply for backlight cathode
2	LEDA	P	Power supply for backlight anode
3	GND	P	Power Ground
4	VCI	P	Power supply for analog circuits
5	GND	P	Power Ground
6-11	R2-R7	I/O	Red data input
12-17	G2-G7	I/O	Green data input
18-23	B2-B7	I/O	Blue data input
24	GND	P	Power Ground
25	CLK	I	Pixel clock input pin, Negative polarity
26	GND	P	Power Ground
27	RESET	I	The signal will reset the LCM, Signal is active low.
28	HSYNC	I	Hertical sync signal, Negative polarity
29	VSYNC	I	Vorizontal sync signal, Negative polarity
30	DEN	I	Data input enable. Display access is enabled when DE is “H”
31	SDO	O	Serial Data Out
32	LCD_CS	I	Chip select input pin (“Low” enable)，for initial RGB I/F。
33	LCD_SDA	I	Serial in/out signal，for initial RGB I/F。
34	LCD_SCL	I	serial interface clock，for einditgiael oRfGthBeI/SFC
35	GND	P	Power Ground
36	TP_RST	I	The signal will reset the TP, Signal is active low
37	TP_SDA	I/O	I2C data signals for TP
38	TP_SCL	I	I2C clock signals for TP
39	TP_INT	O	Interrupt signals for TP
40	TP_VDD	P	TP_VDD Power Supply for TP

I：Input；O：Output；P：Power

4.2 Block Diagram



5. ELECTRICAL CHARACTERISTICS

5.1 TFT-LCD Panel Driving Section

Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Power Supply1 Voltage	IOVCC	1.65	1.8	3.3	V	-
Power Supply2 Voltage	VCI	2.5	2.8	3.3	V	
Power Supply3 Voltage	TP_VDD	2.6	2.8	3.6	V	
Power Supply1 Current	I_{IOVCC}	-	1	-	mA	Note1
Power Supply3 Current	I_{VCI}	-	40	-	mA	Note1
Power Supply4 Current	I_{TP_VDD}	-	7	-	mA	
LCM Logic High level input voltage	V_{IH}	0.7IOVCC	-	IOVCC	V	-
LCM Logic Low level input voltage	V_{IL}	VSSA	-	0.3IOVCC	V	-
LCM Logic High level output voltage	V_{OH}	0.8IOVCC	-	0.8IOVCC	V	I_{OH}=-1.0mA
LCM Logic Low level output voltage	V_{OL}	VSSA	-	0.2IOVCC	V	I_{OL}=+1.0mA
Panel Power Consumption	P_D	-	0.15	-	Watt	Note1
Module Power Consumption	P_{ALL}	-	0.52	-	Watt	Note1,2

(Ta=+25°C,GND=0V)

Note1:Measurement Conditions (Video Mode): Full Screen Red Pattern,VDD=2.8V,60Hz Refresh.

Note2: P_{ALL}= P_D+ P_{BL}， About P_{BL} information, inference to 5.2 Back Light Driving Section.

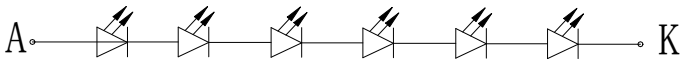
5.2 Back Light Driving Section

Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Forward Voltage	V_F	-	18	-	V	Note1
Forward Current	I_F	-	20	-	mA	Note1
Backlight Power consumption	P_{BL}	-	0.36	-	Watt	Note1
LED life time	-	30000	-	-	Hours	Note2
LED Quantity			6		PCS	

(Ta=+25°C,GND=0V)

Note1: The LED driving condition is defined for each LED module (6 LED Serial, 1 LED Parallel)。
For each LED ： I_F=20mA,V_F=3.2V(Typ.),Ta=25℃。

Note2:The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_{LED}=20mA(Per Led). The LED life time could be decreased if operating I_{LED} is larger than 20mA.

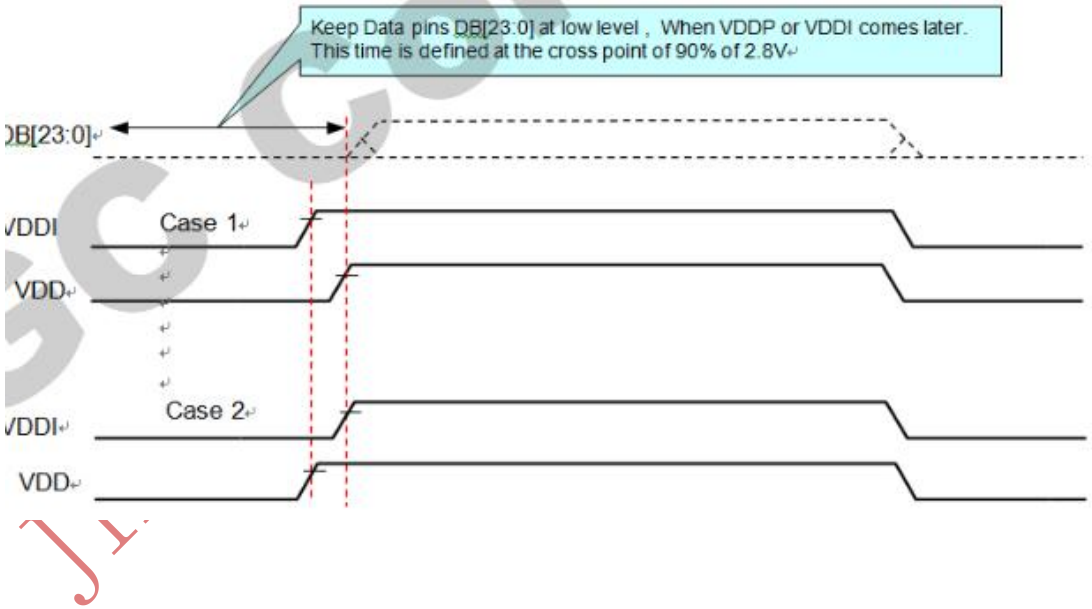


5.3 Power On/Off Sequence

VDDI and VDD can be applied (or powered down) in any order. During the power off sequences, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down with minimum 120msec, and if LCD is in the Sleep In mode, VDD and VDDI can be powered down with minimum 0msec after RESX has been released. CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

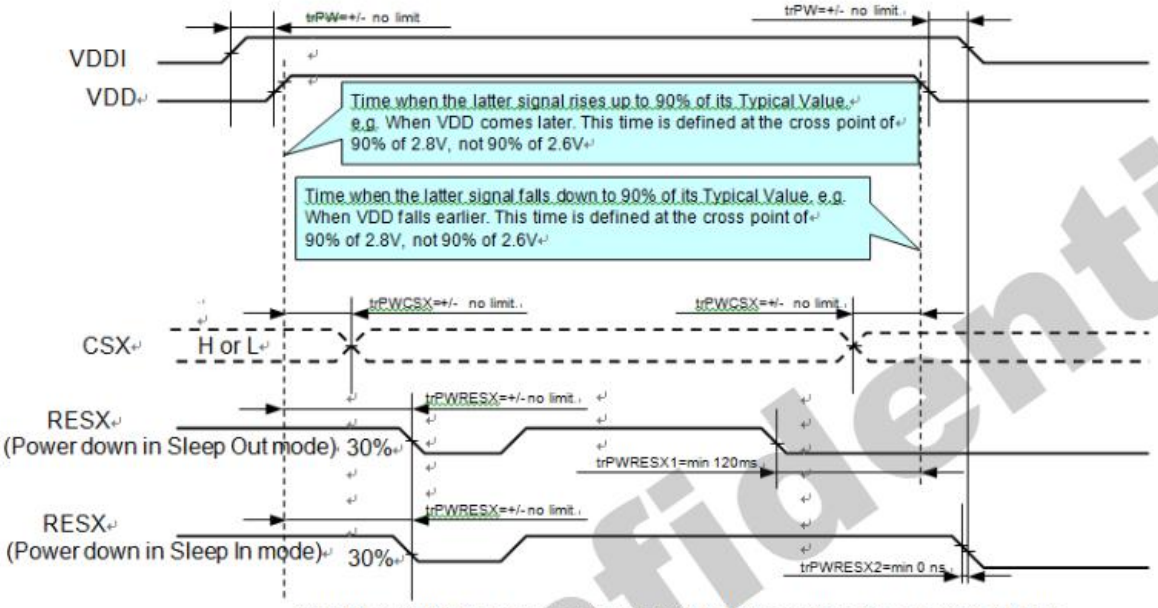
Note:

1. There will be no damage to GC9503CV if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
4. If RESX line is not held stable by host during Power On Sequence as defined in Sections 7.1 and 7.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.
5. Keep data pins DB[23:0] at low level, when VDD or VDDI comes later



5.3.1 RESX line is held High or Unstable by Host at Power ON

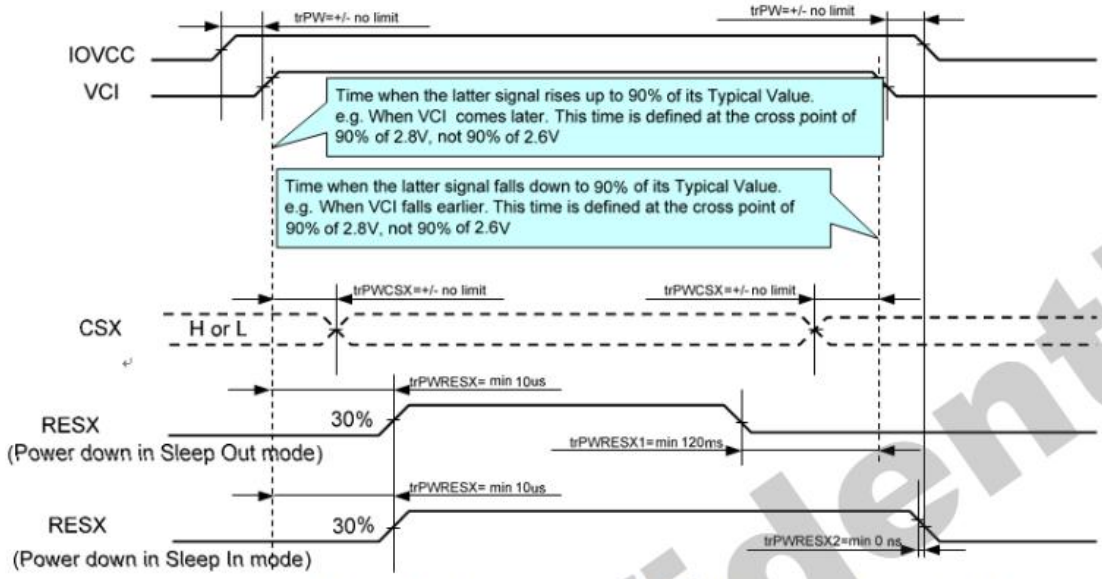
If the RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no
timing restriction upon this hardware reset.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode
trPWRESX2 is applied to RESX falling in the Sleep In Mode

5.3.2 RESX line is held Low by Host at Power ON

If the RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VDD and VDDI have been applied.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode
trPWRESX2 is applied to RESX falling in the Sleep In Mode

Figure 99 Case 2 – RESX line is held Low by Host at Power ON

Note: 1. Unless otherwise specified, timings herein show cross point at 50% of signal power level.

5.3.3 Abnormal Power Off

The abnormal power off means a situation when e.g. there is removed a battery without the normal power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an abnormal power off event, GC9503CV will force the display to blank and will not be any abnormal visible effects with in 1 second on the display and remains blank until “Power On Sequence” powers it up

5.3.3 TP

Reset should be pulled down to be low before powering on and powering down. I2C shouldn’ t be used by other devices during Reset time after VDD powering on (Trtp). INT signal will be sent to the host after ini- tializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Tpdt is more than 1ms.

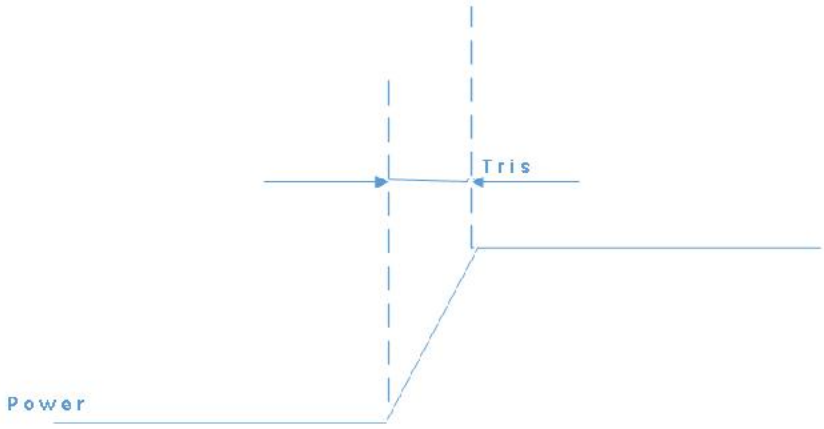


Figure 8.1 power on time

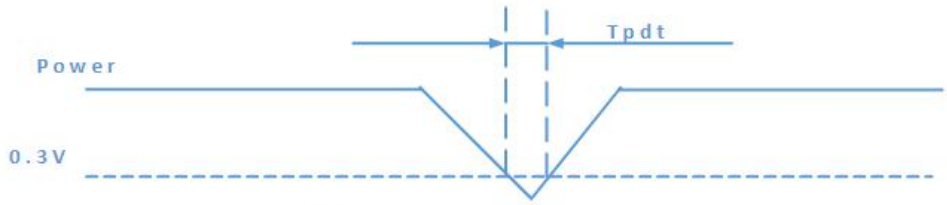


Figure 8-2 Power Cycle requirement

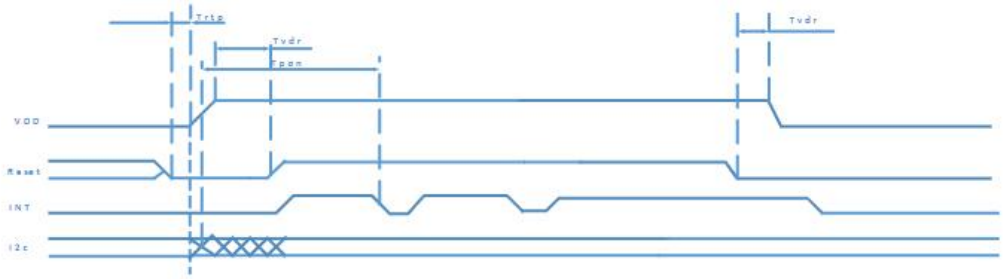


Figure 8-3 Power on Sequence

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

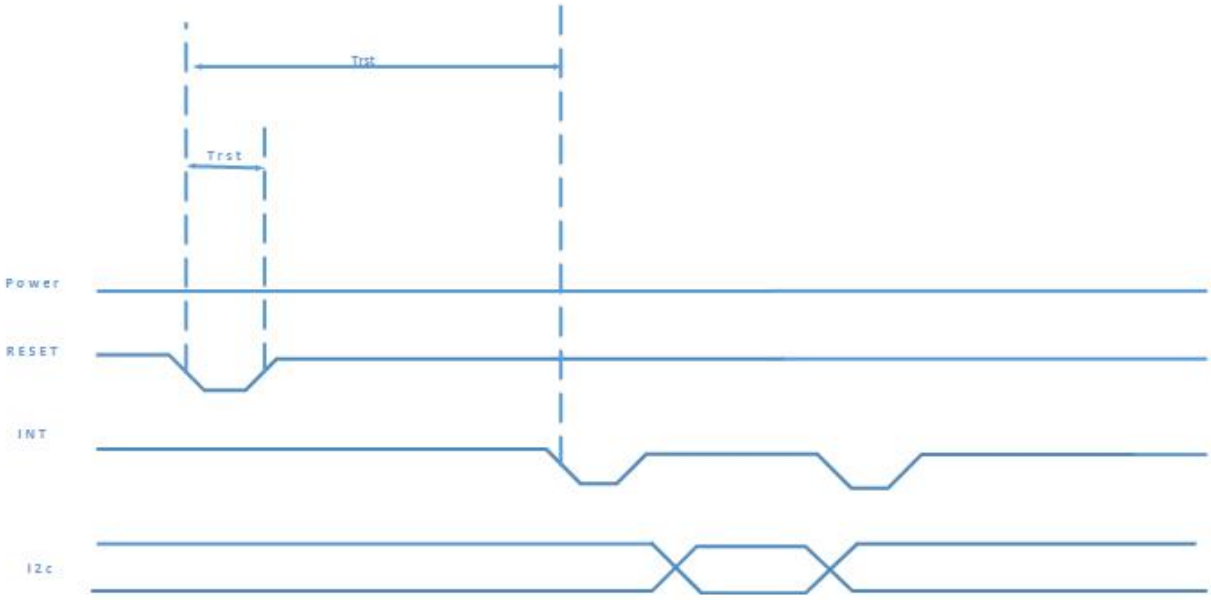


Figure 8.4 Reset Sequence

Table 8-1 Power on/Reset Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	--	5	ms
Tpdt	Time of the voltage of supply being below 0.3V	2	--	ms
Trtp	Time of resetting to be low before powering on	100	--	μs
Tpon	Time of starting to report point after powering on	--	200	ms
Tvdr	Reset time after VDD powering on	1	--	ms
Trsi	Time of starting to report point after resetting	--	200	ms
Trst	Reset time	500	--	us

5.4 Timing Characteristics

5.4.0 TP I2C interface timings

Table 10- 4 AC Characteristics

Parameter	Sym.	Min	Typ.	Max	Unit	Condition
Digital inputs/outputs						
Input high voltage	VIH	0.7VDD		VDD	V	
Input low voltage	VIL	VSS		0.3VDD	V	
Output high voltage	VOH	VDD-0.3		VDD	V	
Output low voltage	VOL	VSS		0.3	V	
ADC						
Differential nonlinearity	DNL		0.6		LSB	
Integral nonlinearity	INL		2		LSB	
Effective number of bits	ENOB		10.5		bit	
Signal-to-noise and distortion ratio (f_{in}=1kHz, f_S=16kHz)	SINAD		65		dB	
Spurious free dynamic range (f_{in}=1kHz, f_S=16kHz)	SFDR		84		dB	

Parameter	Sym.	Min	Typ.	Max	Unit	Condition
Sampling frequency	F_S			2	MHz	VDD reference
				1	MHz	Vbg reference
48MHz RC oscillator						
Nominal frequency	f_{NOM}		48		MHz	
Frequency tolerance	f_{TOL}		1		%	On chip calibration
32kHz RC oscillator						
Nominal frequency	f_{NOM}		32		kHz	
Frequency tolerance	f_{TOL}		0.5		%	On chip calibration

5.4.1 LCM

SPI-8BIT/9BIT Write Cycle Sequence

In write mode of the interface, the host writes commands and data to the GC9503CV. The 3-line serial data packet contains a D/C (data/command) select bit and a transmission byte. If the D/C bit is "low", the transmission byte is interpreted as a command byte. If the D/C bit is "high", the transmission byte is stored in the command register as a parameter data.

Any instruction can be sent in any order to the GC9503CV and the MSB is transmitted first. The serial interface is initialized when the CSX status is high. In this state, SCL clock pulse and SDI data are ineffective. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detail of data format for 3-line serial interface.

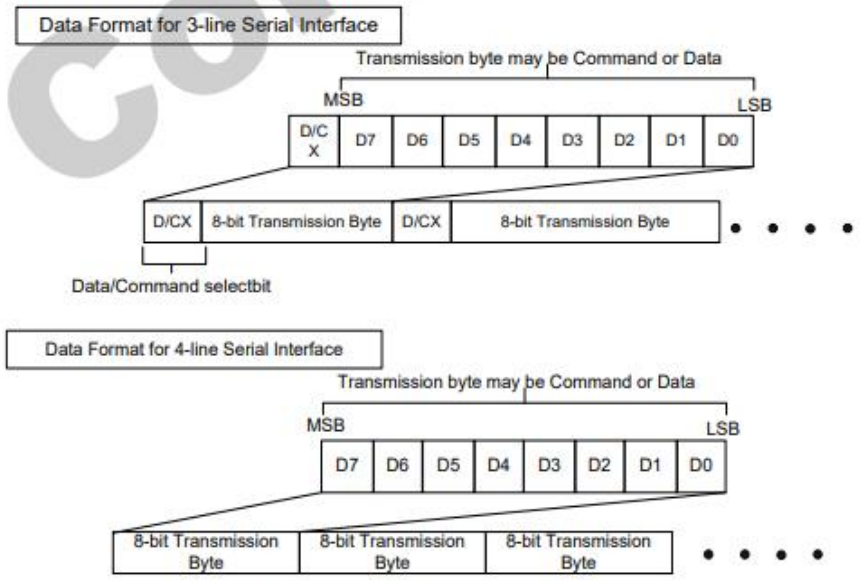


Figure 2 DBI data format

The host drives the CSX pin to low and setting the D/C bit on the SDI pin. The bit is read by the GC9503CV on the first rising edge of the SCL signal. On the next falling edge of the SCL, the MSB data bit (D7) is set on the SDI pin by the host. On the next falling edge of the SCL, the next bit (D6) is set on the SDI pin. If the

SPI-8BIT/9BIT Read Cycle Sequence

optional D/C signal is used, a byte is eight read cycles long. The 3-line serial interface writes sequences described in the Figure 3 below

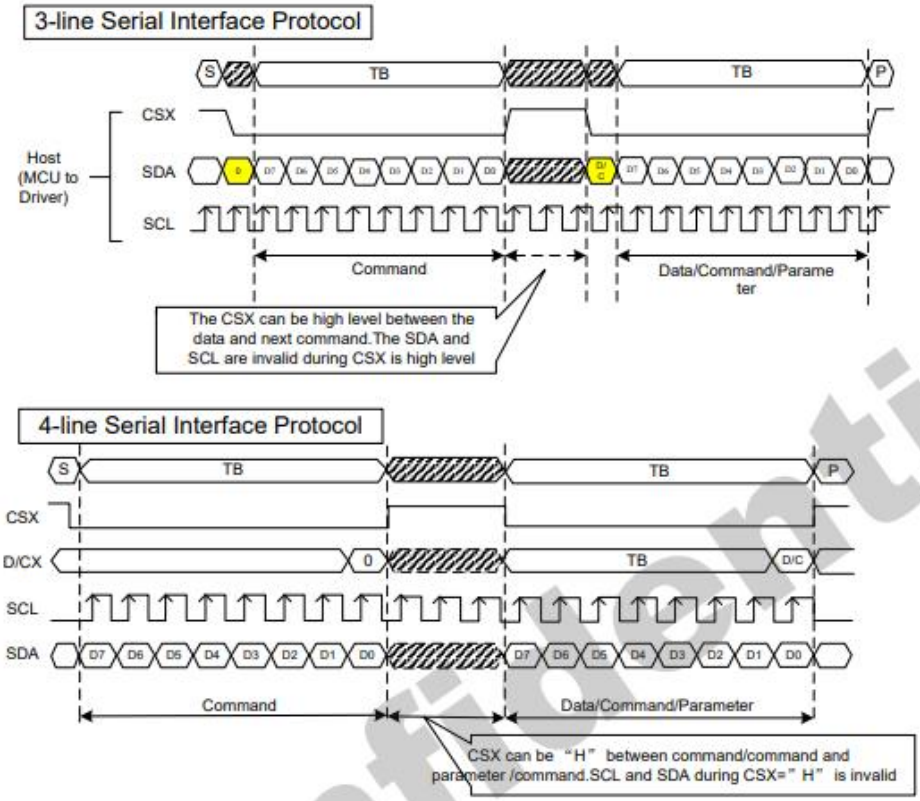
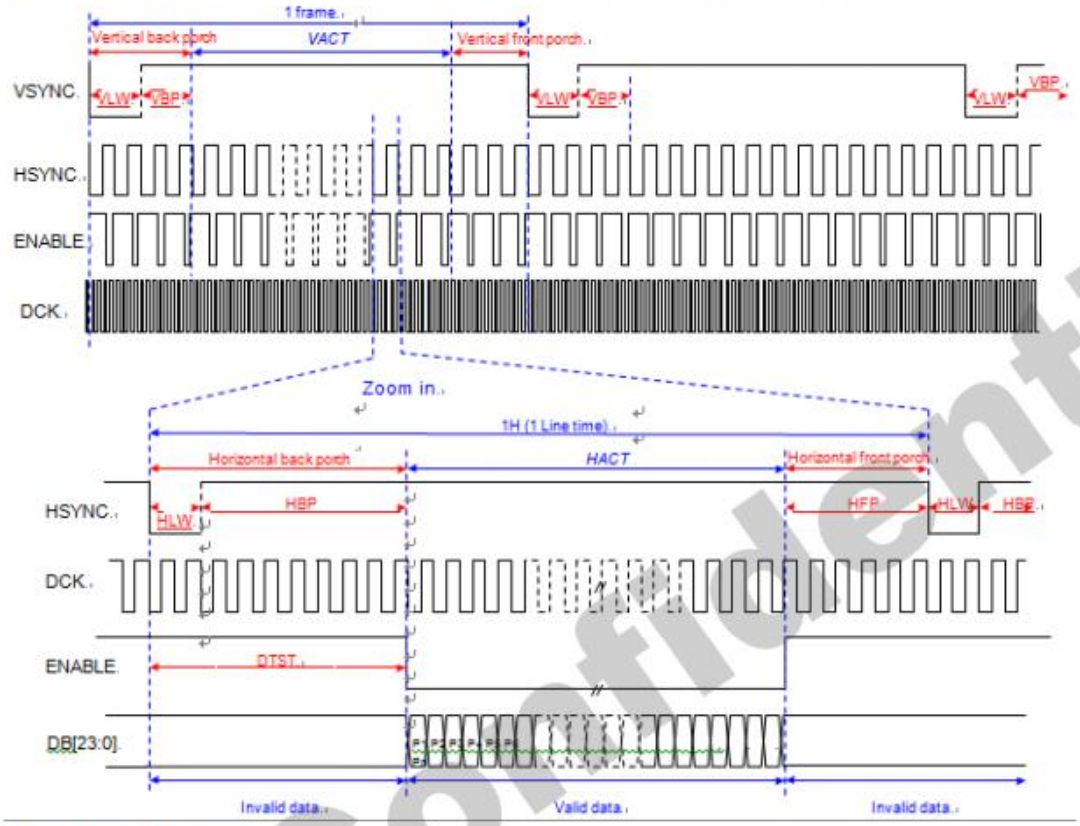


Figure 3 SPI protocol (SCL rising edge example)

DPI Interface Timing

The timing chart of 24-/18-/16-bit DPI (RGB) interface mode is illustrated in Figure 12.



VLW : VSYNC Low pulse Width
HLW : HSYNC Low pulse Width
DTST : Data Transfer Startup Time
Pn : pixel 1, pixel 2…, pixel n

Parameter	Symbols	Condition	Min.	Typ.	Max.	Units
Frame Rate	FR		54		66	fps
Horizontal Low Pulse width	HLW		1		-	DOTCLK
Horizontal Back Porch	HBP		2		126	DOTCLK
Horizontal Address	HACT			480		DOTCLK
Horizontal Front Porch	HFP		2		-	DOTCLK
Vertical Low Pulse width	VLW		1		126	Line
Vertical Back Porch	VBP		1		126	Line
Vertical Address	VACT				960	Line
Vertical Front Porch	VFP		1		255	Line
Data Clock	DCLK		16.6		35.7	MHz

Figure 12 DPI Interface Timing diagram

Note1. HLW+HBP+HFP >= 4.5us.
Note2. VSPL='0', HSPL='0', DPL='0' and EPL='0' of "(Interface Mode Control 21h of the Page 1)" command.

Display Data Format

18bit / pixel 262K colors order on the DPI Interface

The 18-bit RGB interface is selected by setting the DPI[2:0] bits to "110". The display operation is synchronized with VS, HS and PCLK signals.

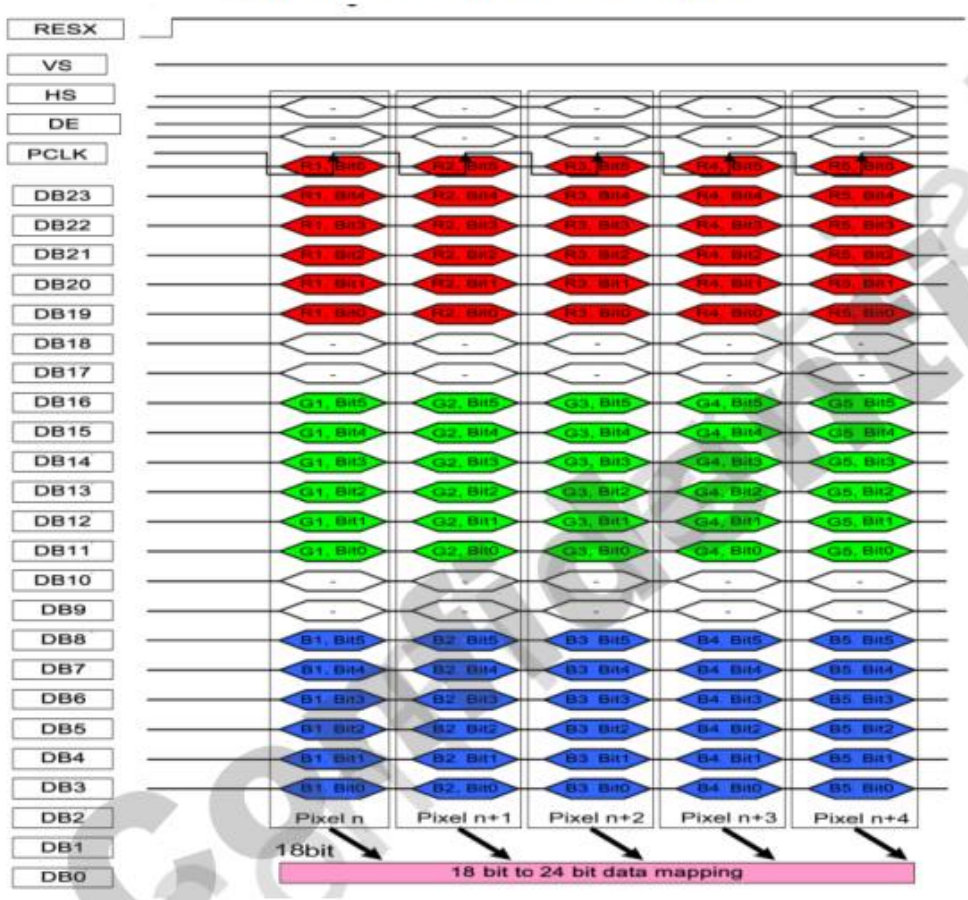


Figure 87 18-bit / pixel 262K colors order on the DPI Interface

Note:

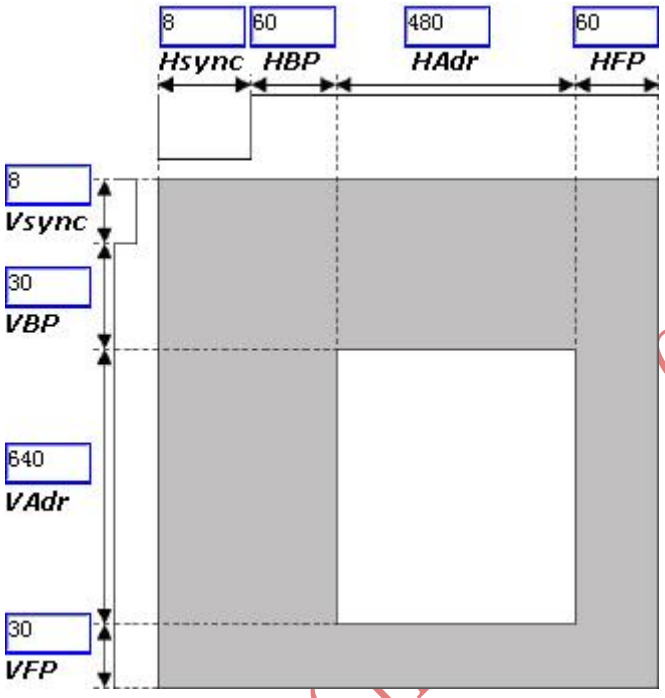
The data order is as follows, MSB=DB23, LSB=DB0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, Red and Blue data.

1-times transfer is used to transmit 1 pixel data to the 18-bit color depth information.

1-

'-'= void

5.5 Timing Diagram



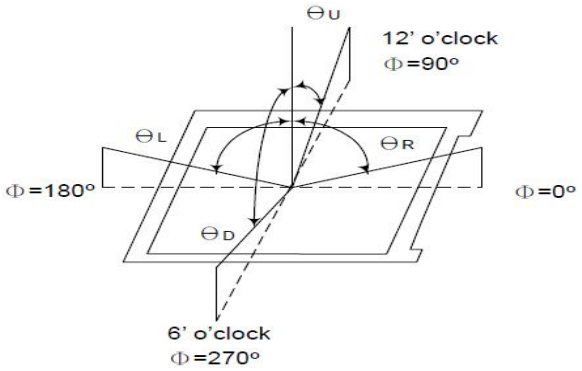
6. OPTICAL CHARACTERISTICS

Parameter 参数	Symbol 符号	Condition 条件	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Contrast Ratio	C/R	θ = 0°	600	800	-	-	Note(4)
NTSC Ratio	S	θ =0°	54	60	-	%	Note(7)
Luminance	L	θ =0°	230	280	-	cd/m2	Note(5)
Luminance uniformity	U_W	θ =0°	-	80	-	%	Note(3)
Response Time	T_R+ T_F	25 °C	-	30	45	ms	Note(2)
Color Coordination	W_X	θ = 0° (Center) Normal viewing angle B/L On	-0.04	TBD	+0.04	NTSC (x,y)	Note(6)
	W_Y			TBD			
	R_X			0.647			
	R_Y			0.329			
	G_X			0.279			
	G_y			0.550			
	B_X			0.134			
	B_Y			0.123			
Viewing Angle	Θ_1	C/R>10	-	80	-	Degree	Note(1)
	θ_R		-	80	-		
	θ_U		-	80	-		
	θ_D		-	80	-		

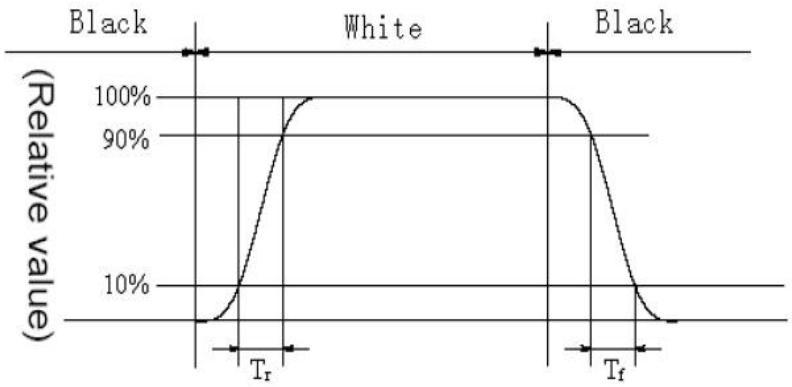
Test Conditions:

1. The ambient temperature is+25℃.
2. The test systems refer to Note 8.

Note1: Definition of Viewing Angle: The viewing angle range that the CR>10

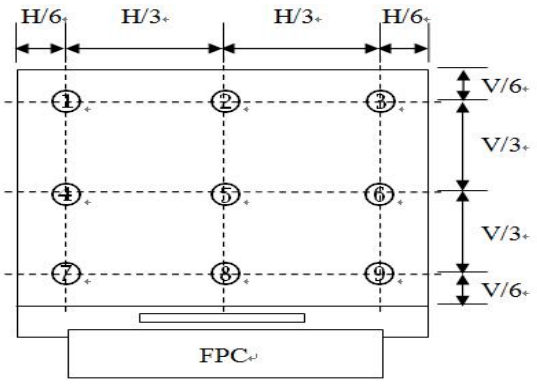


Note2: Definition of Response time: Sum of T_R and T_F



Note 3: Definition of Luminance Uniformity: Active area is divided into 9 measuring areas, every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity} = \frac{\text{Min Luminance of white among 9-points}}{\text{Max Luminance of white among 9-points}} \text{ x100\%}$$



Note4: Definition of Contrast Ratio (CR): measured at the center point of panel

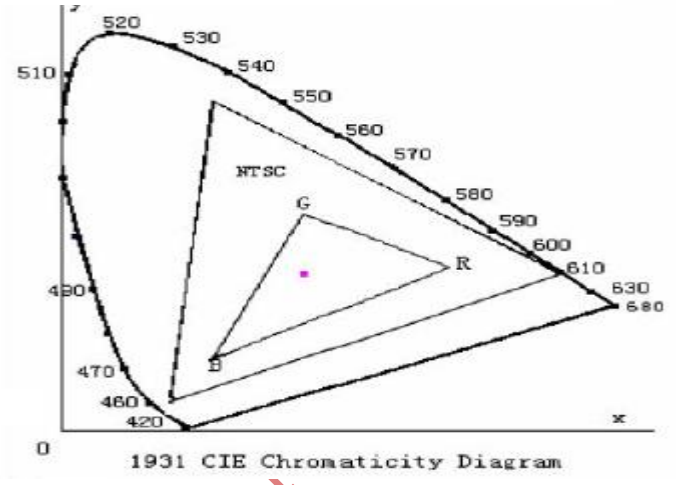
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5 Definition of Luminance: Center Luminance of white is defined as luminance values of 1point average across the LCD surface.

Note 6: Definition of Color Chromaticity (CIE 1931)
Color coordinates of white & red, green, blue measured at center point of LCD.

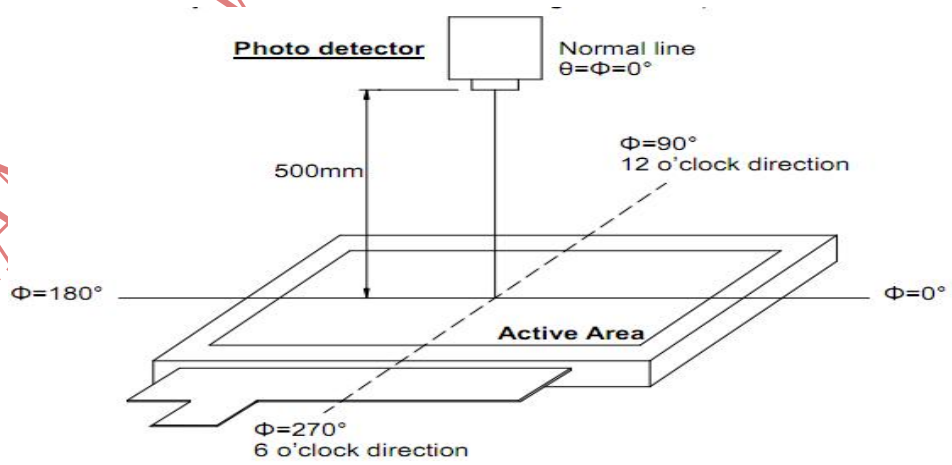
Note 7: Definition of NTSC ratio:

$$\text{NTSC ratio} = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}}$$



Note 8: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen.(Response time is measured by Photo detector TOPCON BM-7, Field of view: 1°/Height: 500mm.)



7. RELIABILITY

Item 项目	Test Condition 测试条件	Remark 备注
High Temperature Storage	Ta =+80°C / 96Hours	Note1,2,3
Low Temperature Storage	Ta =-30°C / 96Hours	Note1,2,3
High Temperature Operating	Ta =+70°C / 96Hours	Note1,2,3
Low Temperature Operating	Ta =-20°C / 96Hours	Note1,2,3
Temperature Cycle storage Test	-40°C/30min Δ+80°C /30min for 30cycles,Transfer time less than 5min	Note2,3
Thermal humidity storage Test	60°C x 90%RH / 96Hours	Note2,3
Package Vibration Test	Frequency: 10Hz~55Hz,Amplitude:1.5mm, 1 hrs for each direction of X, Y, Z	Note2
Packing shock test	Drop to the ground from 60cm height, 1 corner, 3 edges, 6 surfaces.	Note2

Inspection after Test:

Note1:Ta is the ambient temperature of samples.

Note 2: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but doesn't guarantee all the cosmetic specification.

Note 3: Before cosmetic and function tests , the product must have enough recovery time, at least 2 hours at room temperature.

8. PACKAGE DRAWING