

LCD MODULE SPECIFICATION

Model:	UE020QV-RC40-L006F
Version:	V1.0
Date:	2020-06-03

- ☒ **Preliminary Specification** 样品规格书
- ☐ **Final Specification** 量产规格书

Customer Confirmation 客户确认

Approved by	Notes

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VIEWE Confirmation 优奕确认

Prepared by	Reviewed by	Approved by

REVISION HISTORY

Revision 版本号	Date 日期	Contents of Revision Change 修改内容	Remark 备注
V1.0	2019.07.15	Preliminary release	All
V2.0	2019.09.11	Modification of POL and FPC Single Layer Zone and EMI Zone	
L006F	2020.06.02	Replace glass to GTN5020G91CB	

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1. GENERAL INFORMATION

1.1 Features

- 1) Pixel Arrangement: RGB Vertical Stripe
- 2) Interface Mode: SPI 3wire+ RGB 6bits
- 3) Driver IC: ILI9342C
- 4) Operation Temperature: -30~70℃
- 5) Storage Temperature: -40~80℃
- 6) Backlight Type: White LED
- 7) Display mode: Normally White,
- 8) Pixel Density: 200 PPI
- 9) LED life time: 30,000 Hours

1.2 Mechanical Specification

Item 项目	Specification 规格	Unit 单位	Remark 备注
Pixel Driving element	A-Si TFT	-	-
Screen Size	2.0	Inch	Diagonal
Resolution	320(W)*3(RGB)*240(H)	Dots	
Interface	SPI 3wire+ RGB 6bits	-	30PIN
Module Power Consumption	0.3	Watt	Typ.
Active Area	40.80(W)*30.60(H)	mm	-
Pixel pitch (W*H)	0.1275(W)*0.1275(H)	mm	-
Module Size (W*H*D)	46.22(W)*41.03(H)*2.6(D)	mm	-
Luminance	470	cd/m ²	Typ.
Viewing Direction	12	O'clock	-
Display Color	262K	Colors	-

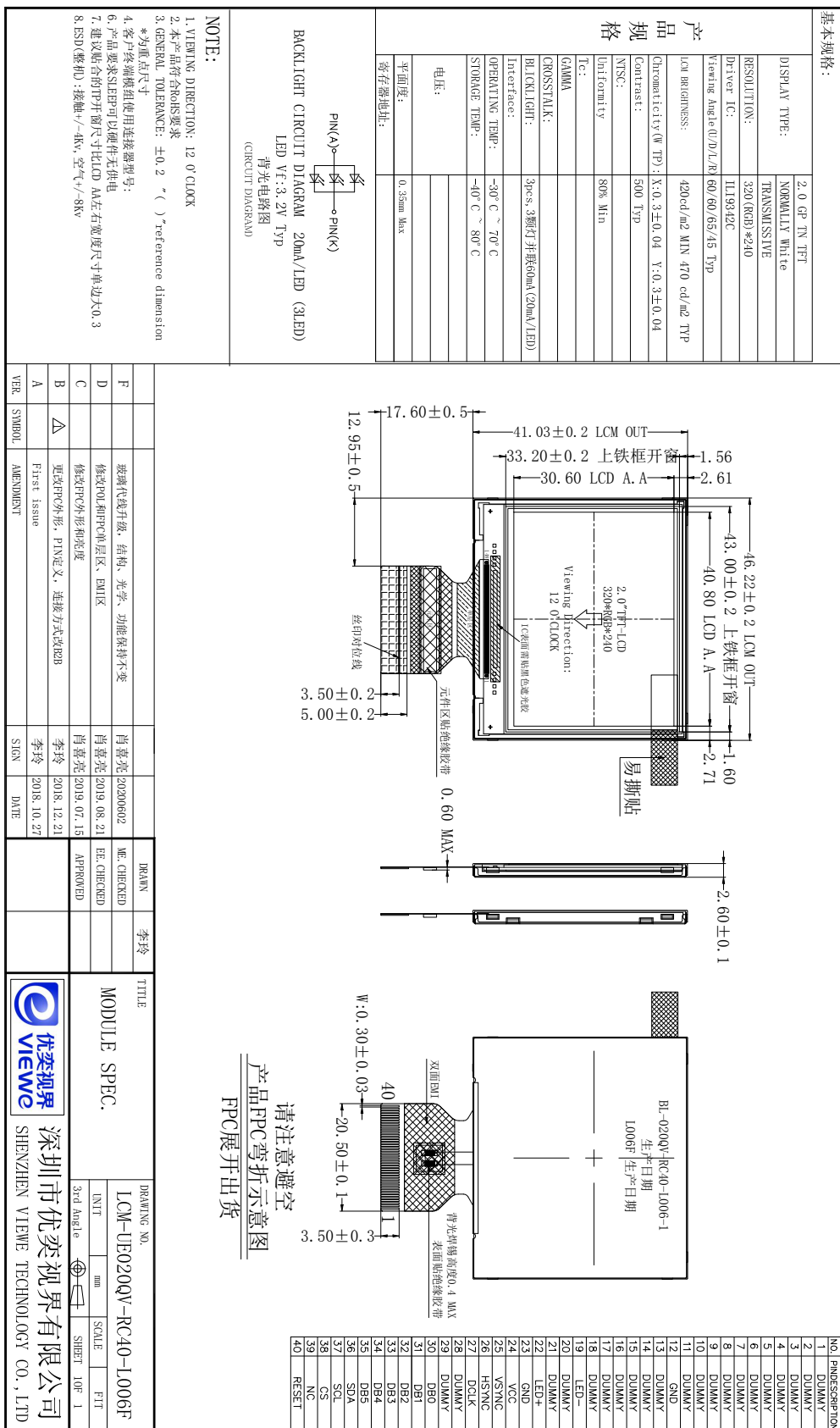
2. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Operating temperature	Top	-20-70	℃
Storage temperature	Tst	-30-80	℃
Input voltage	Vin	-0.3-4.6	V
Supply voltage for logic	VCC	-0.3-4.6	V
Driver supply voltage	VGH - VGL	0-30.0	V

NOTE:

1. If the module is used above these absolute maximum ratings. It may become permanently damaged. Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability.
2. VCC>GND must be maintained.

3. MECHANICAL DRAWING



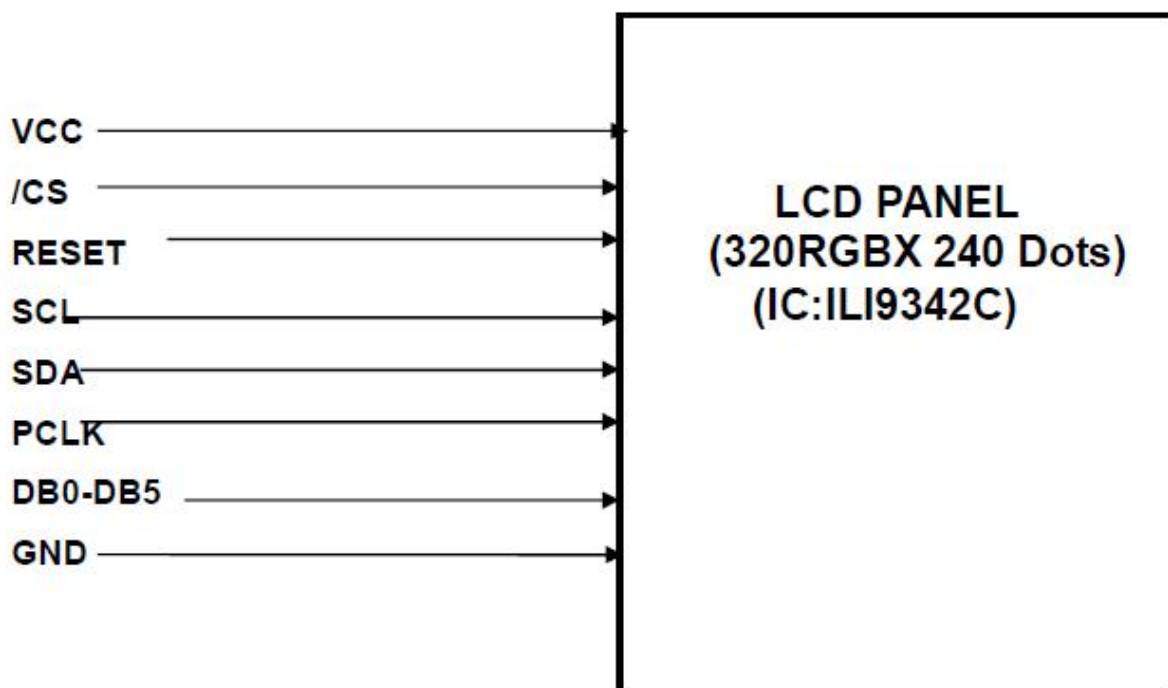
4. I/O CONNECTION & BLOCK DIAGRAM

4.1 I/O Connection

Pin No. 序号	Symbol 符号	I/O	Description 描述
1-11	NC	-	Dummy
12	GND	P	Ground
13-18	NC	-	Dummy
19	LEDK	P	Power supply for backlight cathode
20-21	NC	-	Dummy
22	LEDA	P	Power supply for backlight anode
23	GND	P	Ground
24	VCC	P	Power supply for analog circuit.
25	VSNC	I	Vertical sync signal, default is negative polarity
26	HSNC	I	Horizontal sync signal, default is negative polarity
27	DCLK	I	Pixel clock input pin, default is positive polarity
28-29	NC	-	Dummy
30-35	DB0-DB5		Data input
36	SDA	I/O	Serial communication data input and output
37	SCL	I	Serial communication clock input
38	CS	I	Serial communication chip selectio
39	NC	-	Dummy
40	RESET	I	Global reset pin.

I: Input; O: Output; P: Power

4.2 Block Diagram



5. ELECTRICAL CHARACTERISTICS

5.1 TFT-LCD Panel Driving Section

Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Power Supply1 Voltage	VCC	3.0	3.3	3.6	V	-
Power Supply Current	I _{VDD}	-	30	-	mA	Note1
Logic Input High Voltage	V _{IH}	0.7VCC	-	VCC	V	-
Logic Input Low Voltage	V _{IL}	0	-	0.3VCC	V	-
Panel Power Consumption	P _{VDD}	-	0.099	-	Watt	Note1
Module Power Consumption	P _{LCM}	-	0.3	-	Watt	Note1,2

(Ta=+25°C, DGND=AVSS=0V)

Note1: Measurement Conditions (Video Mode): Full Screen Red Pattern, VDD=3.3V, 60Hz Refresh.

Note2: P_{LCM} = P_{VDD} + P_{BL}, About P_{BL} information, inference to 5.2 Back Light Driving Section.

5.2 Back Light Driving Section

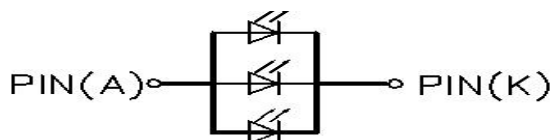
Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Forward Voltage	V _F	-	3.2	-	V	Note1
Forward Current	I _F	-	60	-	mA	Note1
Backlight Power consumption	P _{BL}	-	0.192	-	Watt	Note1
LED life time	-	30000	-	-	Hrs	Note2
LED Quantity		3			PCS	

(Ta=+25°C, DGND=AVSS=0V)

Note1: The LED driving condition is defined for each LED module (1LED Serial, 3 LED Parallel).

For each LED : I_F=20mA, V_F=3.2V(Typ.)/3.4V(Max.), Ta=25°C。

Note2: The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_{LED}=20mA(Per Led). The LED life time could be decreased if operating I_{LED} is larger than 20mA.



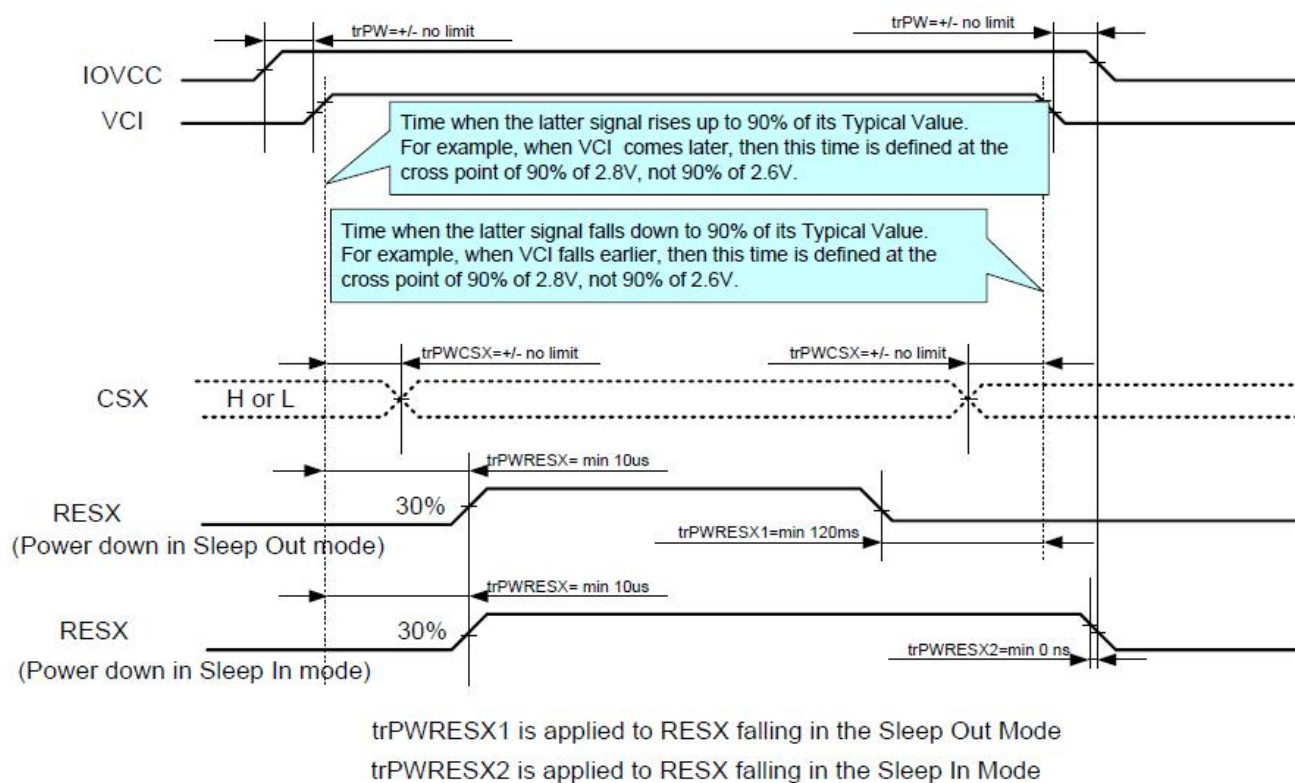
BACKLIGHT CIRCUIT DIAGRAM 20mA/LED (3LED)

LED Vf: 3.2V Typ

背光电路图

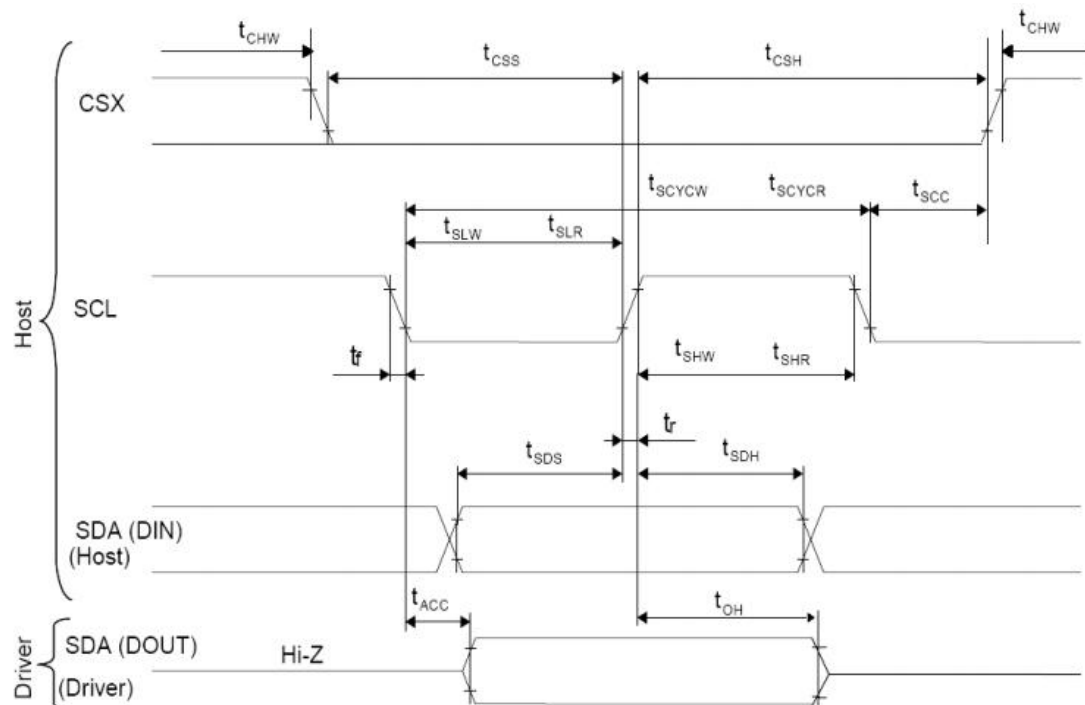
(CIRCUIT DIAGRAM)

5.3 Power On/Off Sequence



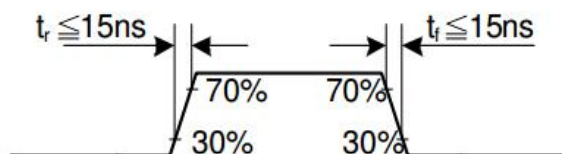
5.4 Timing Characteristics

5.4.1 Serial interface Characteristics (3-line serial)

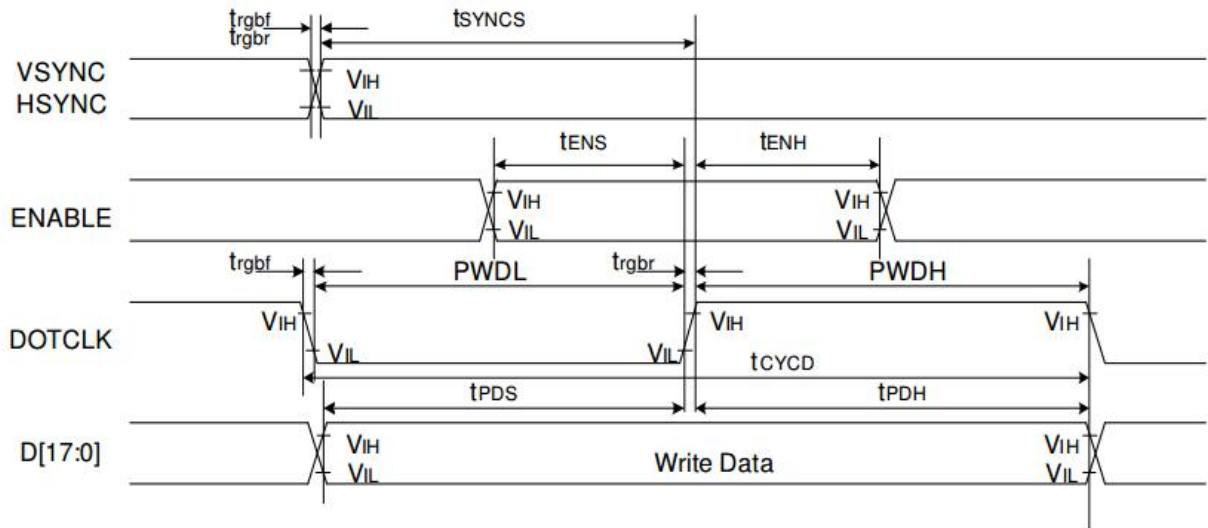


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	35	-	ns	
	tslw	SCL "L" Pulse Width (Write)	35	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	15	50	ns	
CSX	tsc	SCL-CSX	20	-	ns	
	tch	CSX "H" Pulse Width	40	-	ns	
	tcs	CSX-SCL Time(write)	30	-	ns	
	tcs		30	-	ns	

Note: $T_a = 25^\circ\text{C}$, $IOVCC = 1.65\text{V to } 2.8\text{V}$, $V_{CI} = 2.6\text{V to } 3.3\text{V}$, $AGND = GND = 0\text{V}$

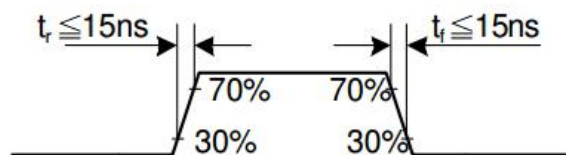


5.4.2 Parallel 18/16/6-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	33	-	ns	18/16-bit bus RGB interface mode
	PWDL	DOTCLK low-level period	33	-	ns	
	t_{CYCD}	DOTCLK cycle time(18 bit)	100	-	ns	
	t_{rgrb}, t_{rgrbf}	DOTCLK, HSYNC, VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	25	-	ns	
	PWDL	DOTCLK low-level pulse period	25	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{rgrb}, t_{rgrbf}	DOTCLK, HSYNC, VSYNC rise/fall time	-	15	ns	

Note: $T_a = -30$ to $70\text{ }^{\circ}\text{C}$, $IOVCC=1.65\text{V}$ to 2.8V , $VCI=2.6\text{V}$ to 3.3V , $AGND=GND=0\text{V}$



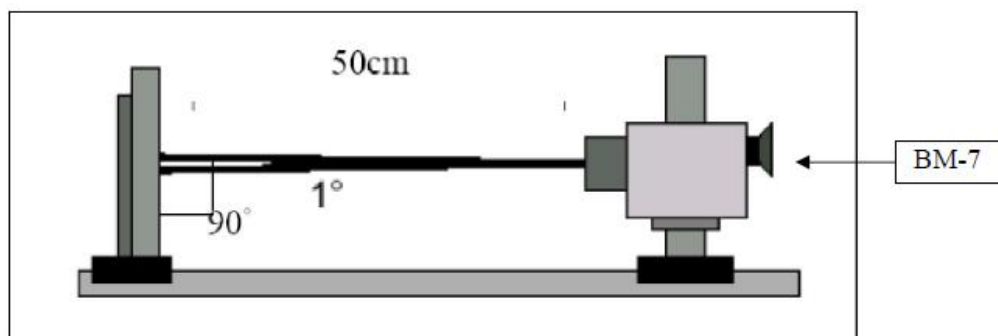
6. OPTICAL CHARACTERISTICS

Parameter 参数	Symbol 符号	Condition 条件	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Contrast Ratio	C/R	$\theta = 0^\circ$	450	500	-	-	Note(3)
NTSC Ratio	S	$\theta = 0^\circ$	-	60.1	-	%	Note(10)
Luminance uniformity	U_W	$\theta = 0^\circ$	70	80	-	%	Note(7)
Response Time	$T_{R+} T_F$	25 °C	-	35	50	ms	Note(4)
Color Coordination	W_X	$\theta = 0^\circ$ (Center) Normal viewing angle B/L On	-0.03	0.313	+0.03	NTSC (x,y)	Note(8)
	W_Y			0.336			
	R_X			0.641			
	R_Y			0.344			
	G_X			0.297			
	G_Y			0.571			
	B_X			0.137			
	B_Y			0.124			
Viewing Angle	θ_L	C/R>10		60	-	Degree	Note(5)
	θ_R			60	-		
	θ_U			60	-		
	θ_D			50	-		

Note 1: Ambient temperature = 25 ± 2 °C;

Note 2: To be measured in the dark room;

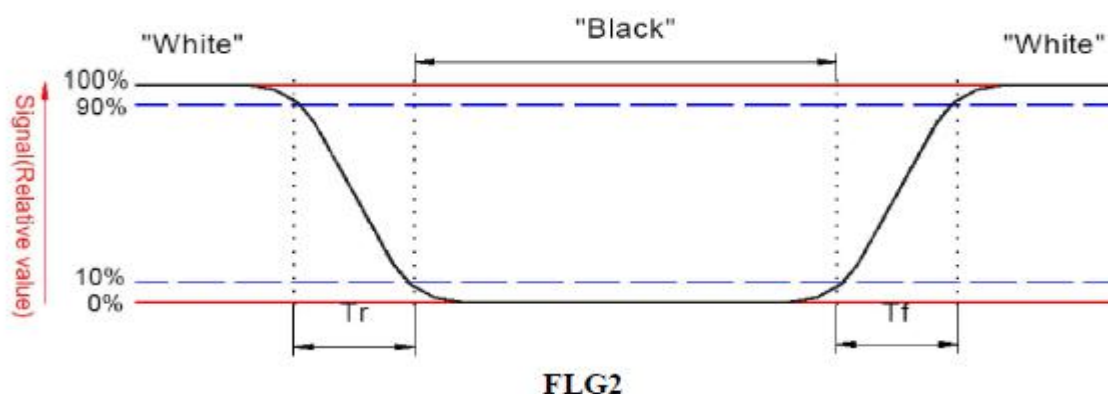
Note 3: To be measured at the center area of the panel with a view cone of 1° by BM-7, after 10 minutes operation (module).



FLG1

Note 4: Define the response time:

The output signals of photo detector are measured when the input signals are charged from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5: Contrast Ratio (CR) is defined mathematically as For more information from FLG3

$$\text{Contrast Ratio} = \frac{\text{Average surface luminance with all white pixel (P1,P2,P3,P4,P5,P6,P7,P8,P9)}}{\text{Average surface luminance with all black pixel (P1,P2,P3,P4,P5,P6,P7,P8,P9)}}$$

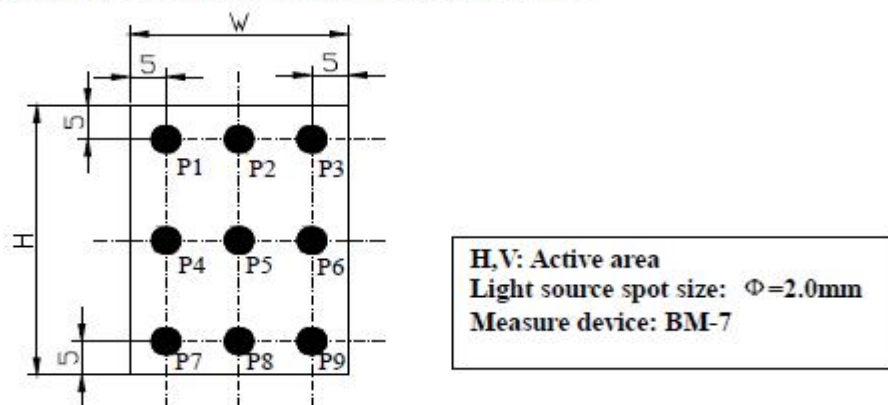
Note 6: Surface luminance is the center point across the LCD surface 500mm from the surface with all pixel displaying white, For more information see the FLG3

$$L_v = \text{Average Surface luminance with all white pixel(P1,P2,P3,P4,P5,P6,P7,P8,P9)}$$

Note 7: The uniformity in surface luminance, δ white is determined by measuring luminance at each test position 1 to 5, and then dividing the maximum luminance of 5 points luminance by minimum luminance of 5 points luminance. For more information see FLG3.

$$\delta \text{ WHITE} = \frac{\text{Minimum surface luminance with all white pixel(P1,P2,P3,P4,P5,P6,P7,P8,P9)}}{\text{Maximum surface luminance with all white pixel(P1,P2,P3,P4,P5,P6,P7,P8,P9)}}$$

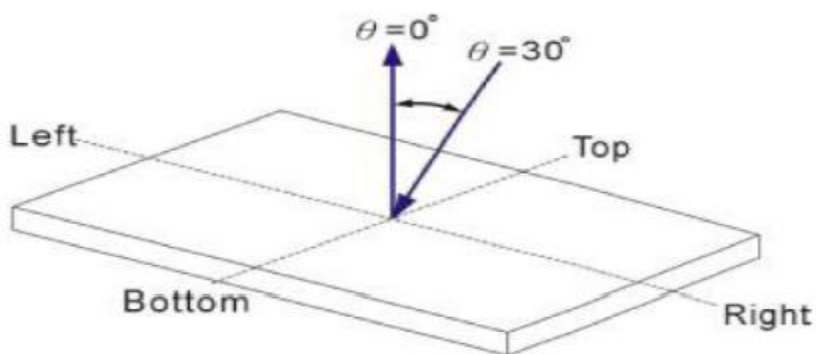
Note 8: CIE(X, Y), the X, Y value is determined by measuring luminance at each test position 1 to 5, and then make average value. For more information see FLG3.



FLG3

Note 9: Viewing angle is the angle at which the contrast ratio is greater than 2, TFT module the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the

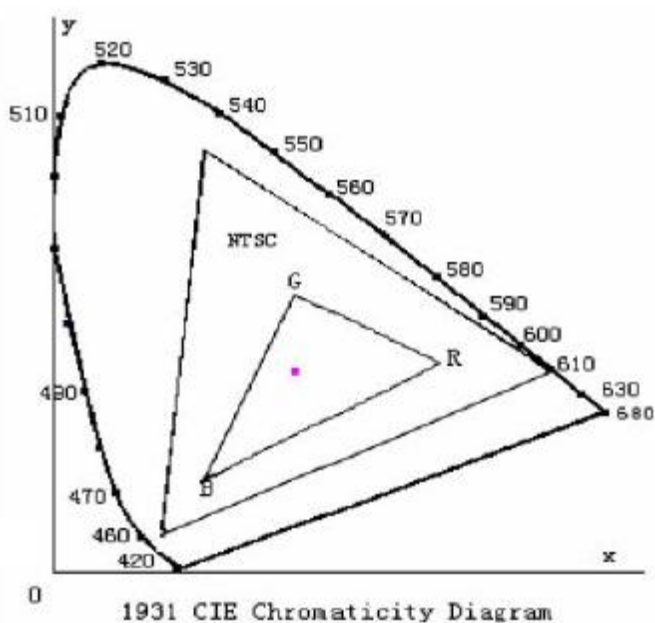
vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see the FLG 4.



FLG4

Note 10: Definition of NTSC ratio:

$$\text{NTSC ratio} = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}}$$



7. RELIABILITY

Item 项目	Test Condition 测试条件	Remark 备注
High Temperature Storage	Ta =+80°C / 240Hours	Note1,2,3
Low Temperature Storage	Ta =-40°C / 240Hours	Note1,2,3
High Temperature Operating	Ta =+70°C / 240Hours	Note1,2,3
Low Temperature Operating	Ta =-30°C / 240Hours	Note1,2,3
Temperature Cycle storage Test	-40°C/30min ↔ +80°C /30min for 30cycles, Transfer time less than 5min	Note2,3
Thermal humidity storage Test	60°C x 90%RH / 240Hours	Note2,3
Package Vibration Test	Frequency: 10Hz~55Hz, Amplitude: 1.5mm, 1 hrs for each direction of X, Y, Z	Note2
ESD	C=150PF, R=330 Ohm Air: ± 8kv, 5times(Center) Contact: ± 4kv, 5times(Center)	Note4

Inspection after Test:

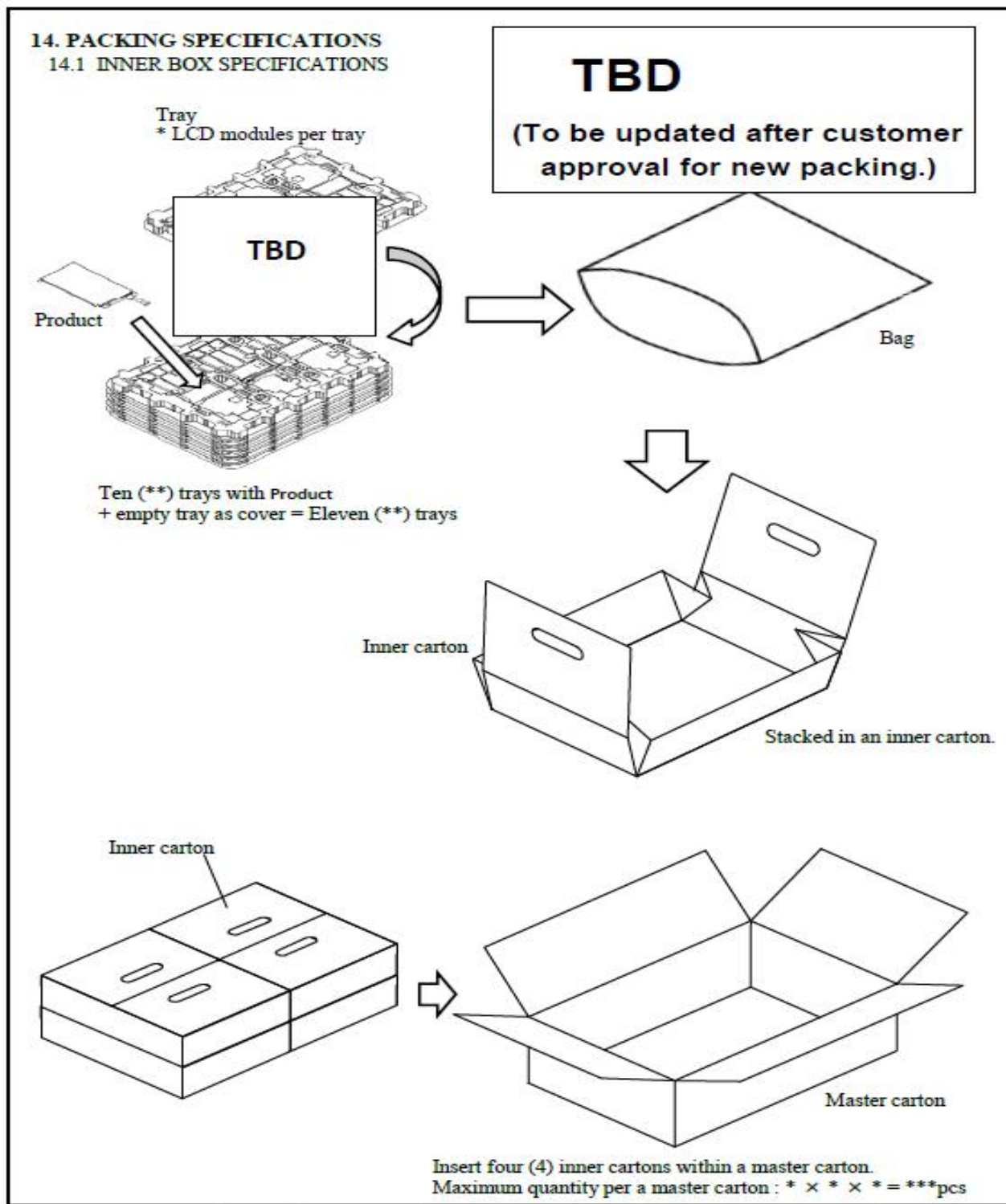
Note1: Ta is the ambient temperature of samples.

Note 2: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but doesn't guarantee all the cosmetic specification.

Note 3: Before cosmetic and function tests, the product must have enough recovery time, at least 2 hours at room temperature.

Note 4: In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

8. PACKAGE DRAWING



10.模组 ROHS 报告附件打包资料